INJECTION TEST:
BUILDING A DATA INJECTOR FOR THE ATLAS LIQUID ARGON SIGNAL PROCESSOR

2022 WINTER NUCLEAR AND PARTICLE PHYSICS CONFERENCE

MAHEYER J. SHROFF
UNIVERSITY OF VICTORIA

FEB 18 2022

ATLAS AT THE LHC

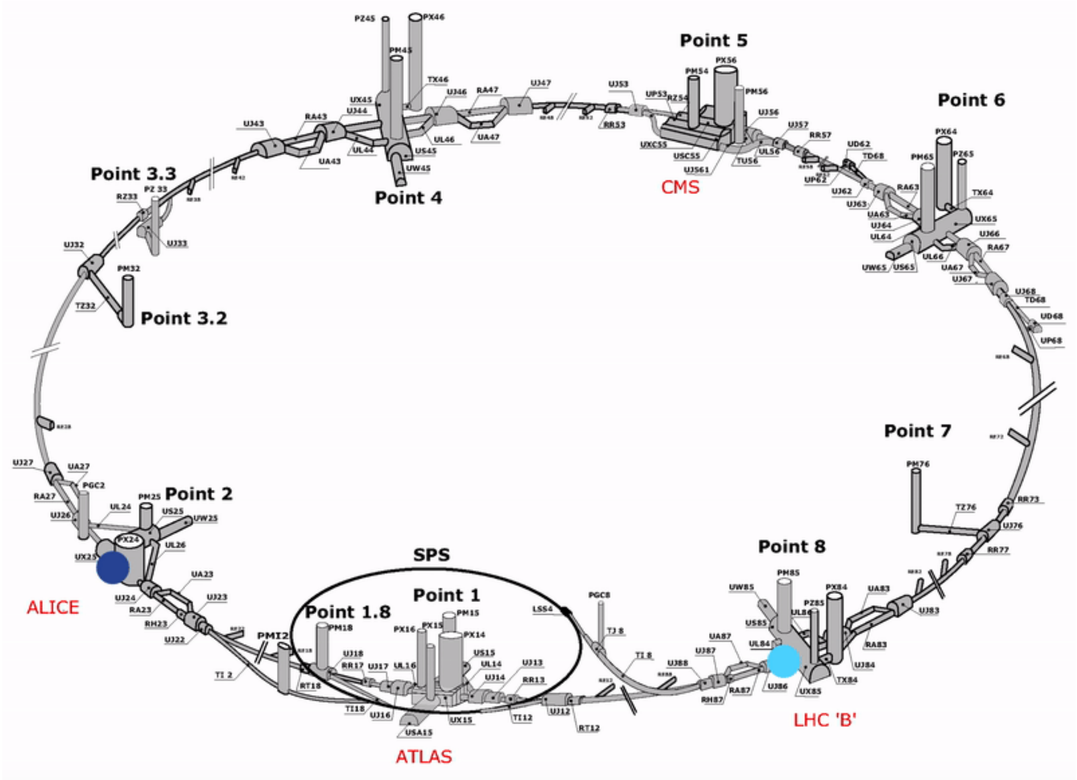
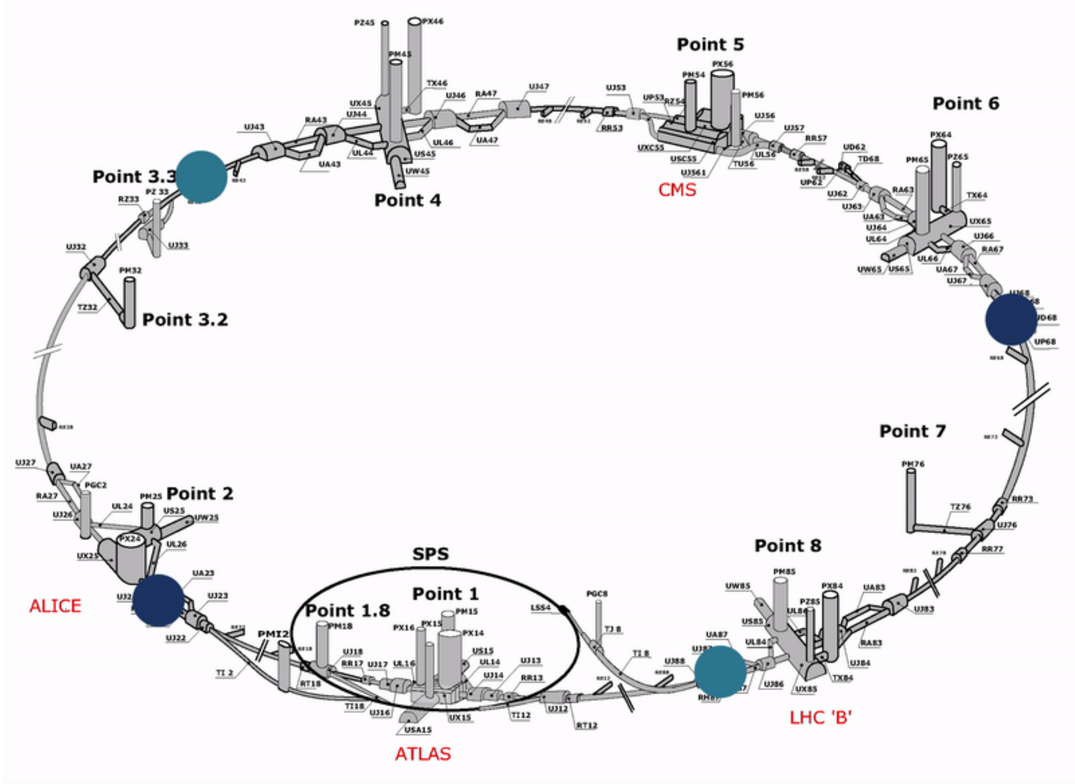


FIG 1: SKETCH OF THE UNDERGROUND LHC ACCELERATOR RING WITH ITS MAIN EXPERIMENTS [1]

- The Large Hadron Collider is a $p-p$ accelerator colliding protons at $\sqrt{s} \sim$ 13 TeV.
- Protons are accelerated in bunches and collide every 25ns with a maximum peak luminosity so far of $2 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$
- The ATLAS detector is a cylindrical multi-purpose detector placed at one of the interaction points around the LHC ring.
- The Large Hadron Collider is due to undergo major design changes with the goal of colliding protons at $\sqrt{s} =$ **14** TeV and with a peak luminosity of up to $7.5 \times 10^{34}\textbf{cm}^{-2}\textbf{s}^{-1}$.

ATLAS AT THE HIGH LUMINOSITY LHC



The HL-LHC increases luminosity by increasing the **number of bunches** as well as the **bunch intensity** of protons in the ring.

FIG 1: SKETCH OF THE UNDERGROUND LHC ACCELERATOR RING WITH ITS MAIN EXPERIMENTS [1]

- As a result, detectors in the LHC ring like ATLAS need to undergo upgrades necessary to maintain good physics performance in the HL-LHC environment.
- One of these upgrades deals with the *LAr calorimeter* system:
  - ✦ Trigger: A higher rate, more discriminating trigger and readout system is needed in a higher pileup environment.
  - ✦ Radiation: Planned radiation dose exceeds capacity of existing readout system

LAr ELECTRONIC UPGRADES

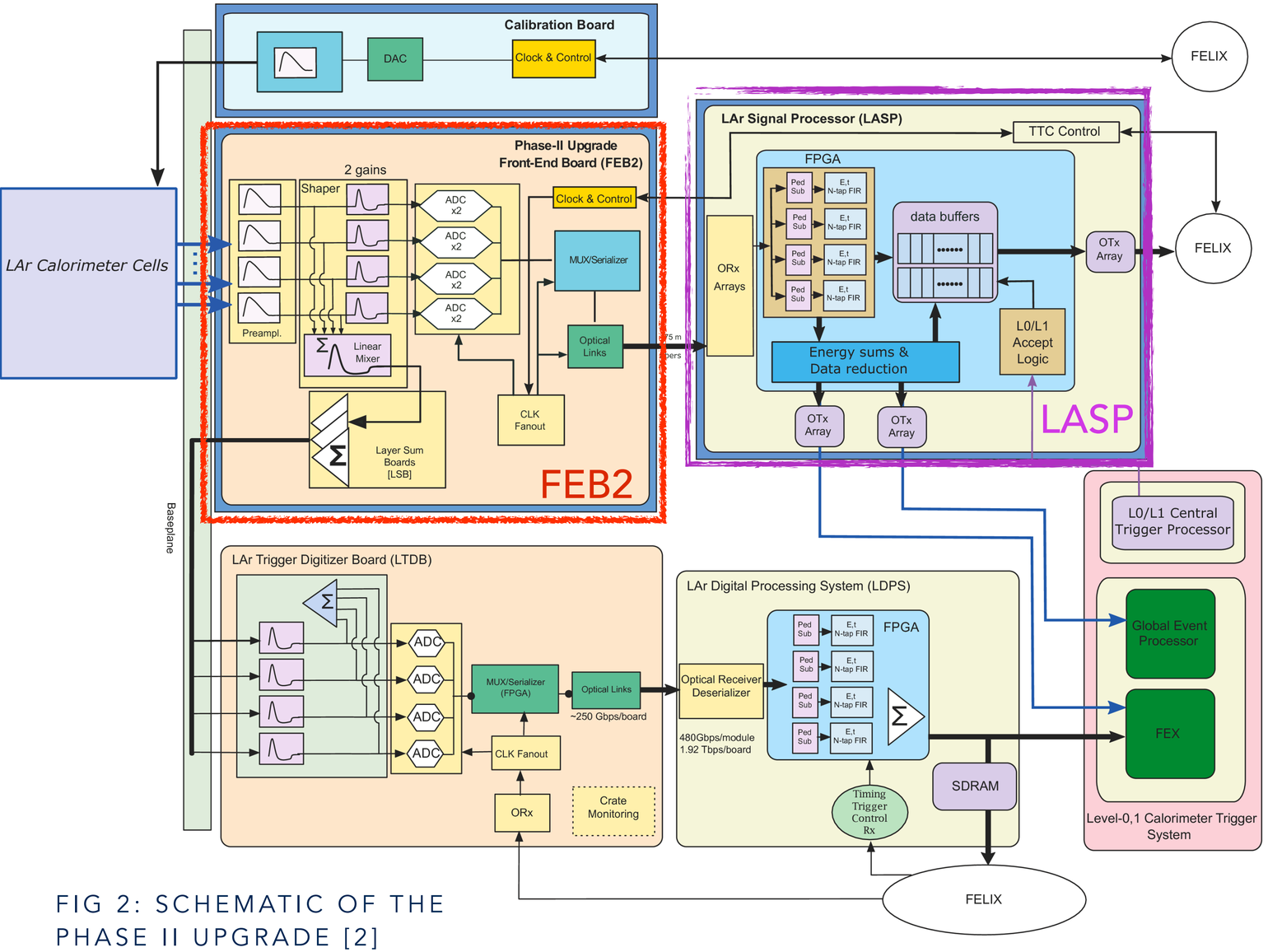


FIG 2: SCHEMATIC OF THE PHASE II UPGRADE [2]

Two major changes are planned for Phase II LAr Electronics upgrade

1 . FEB2 (Front End Board 2)

Signals passed through an analogue filter shaper for two different gains (high & low gain)

↓

ADC digitize this into 16-bit words

↓

A serialized stream is sent to the LASP at 10.24Gbps and 40 MHz using custom CERN-based chips.

2. LASP (LAr Signal Processor)

LASP, **built on an FPGA,** will then

- ✶ calculate energy/time of pulses
- ✶ transmit data to the trigger & DAQ
- ✶ Buffer data until trigger decision

THE NEED FOR AN INJECTOR

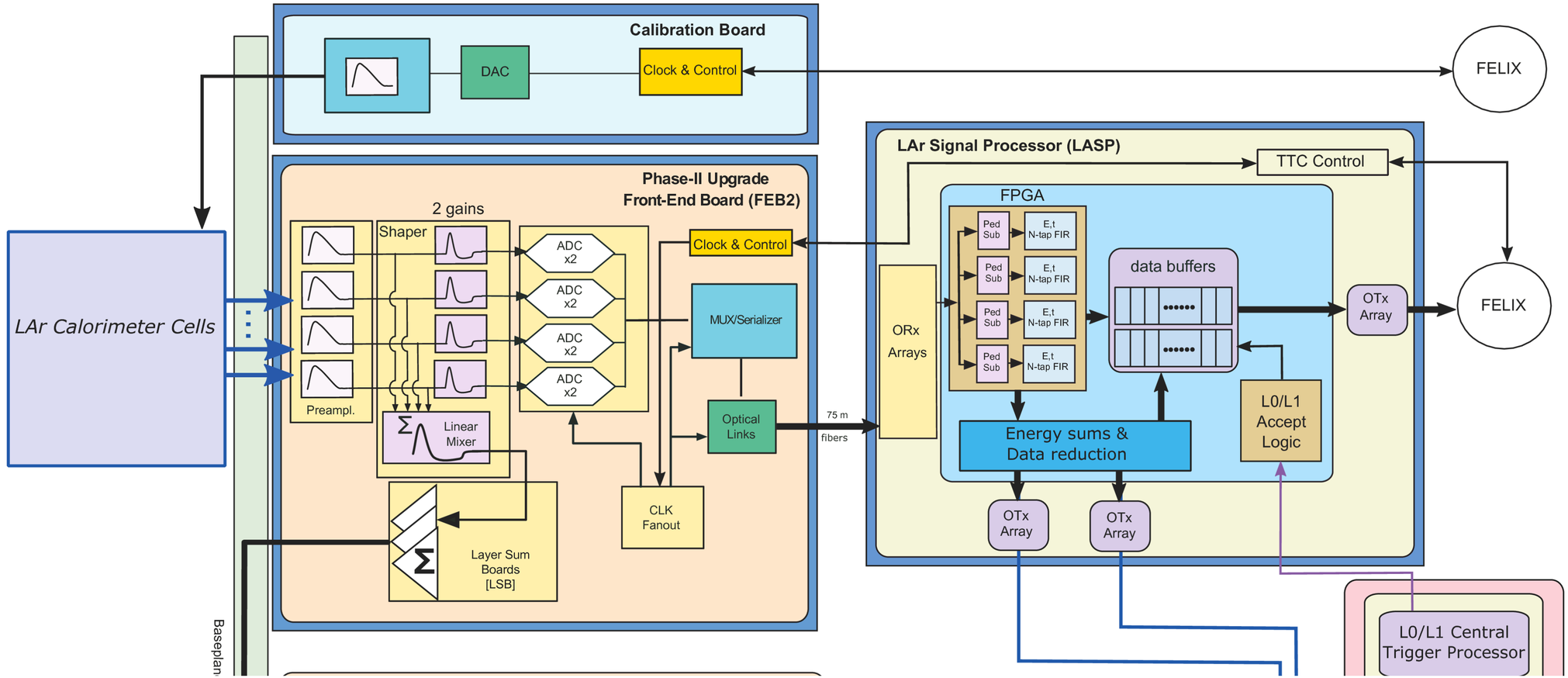


FIG 3: SCHEMATIC OF THE PHASE II UPGRADE (**CROPPED**) [2]

- Signals from the calorimeter and the FEB2 will not be available as the LASP is developed
- Monte Carlo simulations can mimic FEB2 pulses for different physics events
- As the LASP is being developed, it needs to be tested with external test cases to verify operation.

THE NEED FOR AN INJECTOR

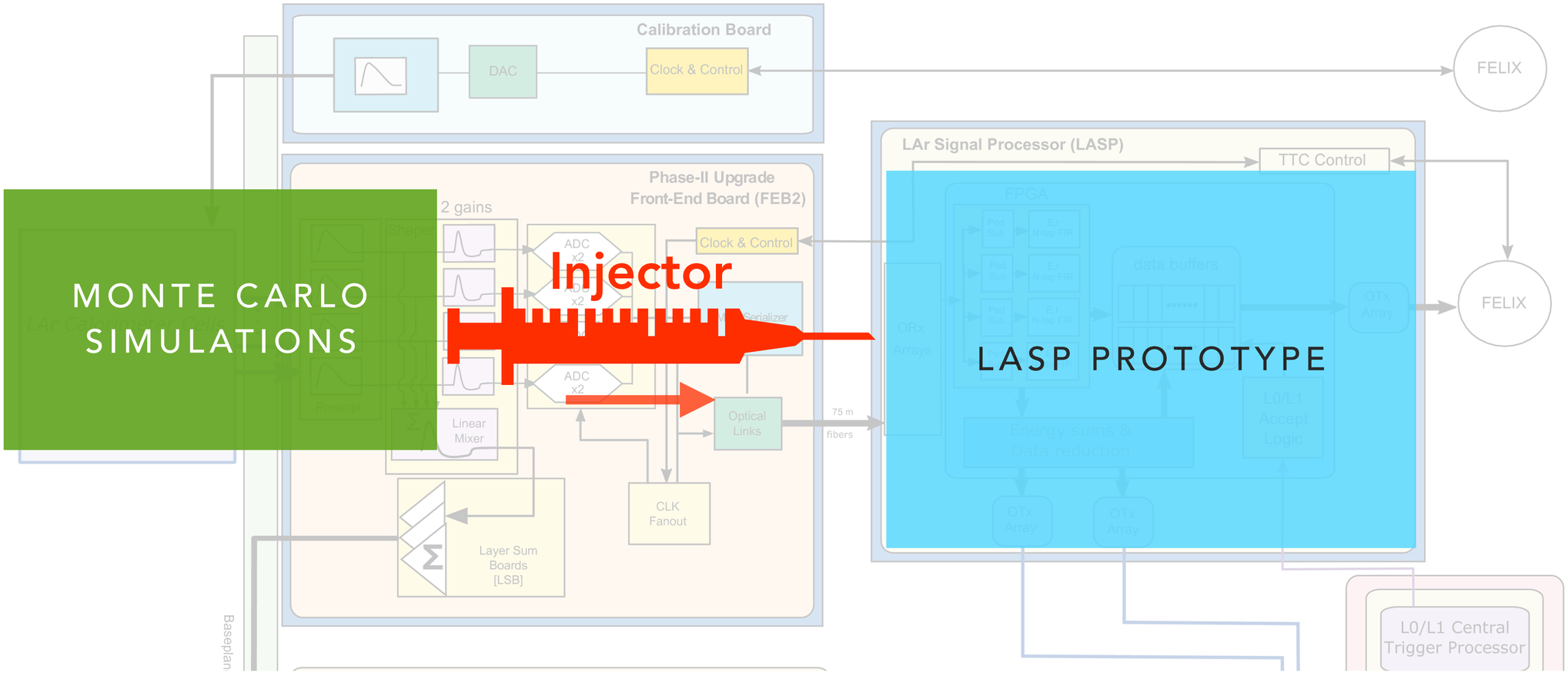


FIG 3: SCHEMATIC OF THE PHASE II UPGRADE (**CROPPED**) [2]

- As the LASP is being developed, it needs to be tested by external test cases to verify operation.
- Thus, we need a data injector that will input pulses similar to those expected from the FEB2s

REQUIREMENTS FOR THE INJECTOR

- The Injector project is an integral part of the LASP test-bench.

SPECIFICATION (SUMMARIZED)

"The data injector shall provide, with the **highest fidelity**, **22 channels** of **FEB2 payloads** transmitted at **10.24 Gbps**. The payload should be **user-controlled** which can help test the LASP for different cases. Data injection should occur for **as long as possible**"

➡ **Highest fidelity:** Ability to maintain transmission accuracy

➡ **22 channels**: 22 independent streams of data

➡ **FEB2 payloads**: payload structure as transmitted by FEB2s i.e. 12 ADCs + 2 BCIDs (Bunch Crossing IDs)

➡ **10.24 Gbps**: FEB2 transmission speed

➡ **User-controlled**: user having the ability to manipulate the values

➡ **As long as possible**: duration of injection

FPGAs

- The Injector (and the LASP) is built on a firmware programmable integrated circuit called an **FPGA** (Field Programmable Gate Array)
- FPGA devices contain logic cells and programmable switches. Logic cells can be programmed to perform functions, while the programmable switches can be customized to provide interconnections between logic cells.
- The Injector is implemented on an Intel Stratix 10 GX FPGA board

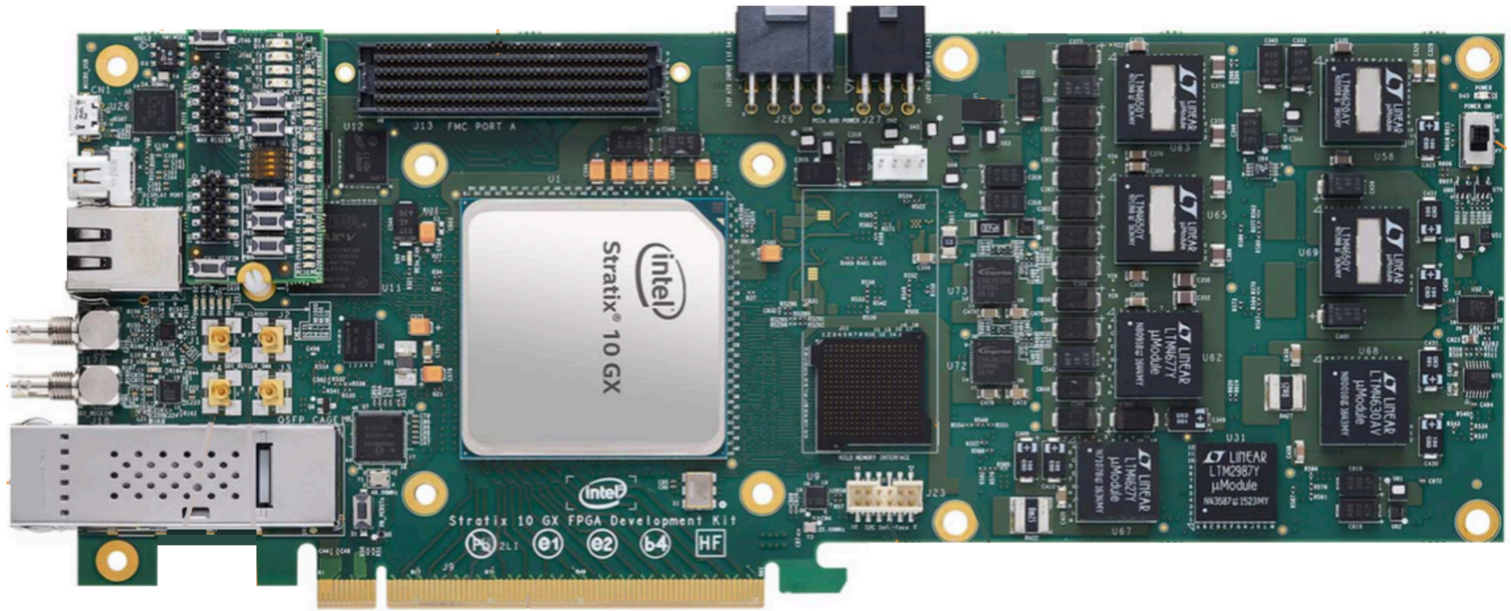


FIG 4: FRONTAL IMAGE OF THE INTEL STRATIX 10 GX BOARD [3]

The Stratix 10 board has the following capabilities which are exploited for the Injector project

- ✓ **100 Gbps transceivers**
- ✓ **1 Gbps Ethernet connector**
- ✓ **2 GB external memory device**

DESIGN SCHEME & IMPLEMENTATION

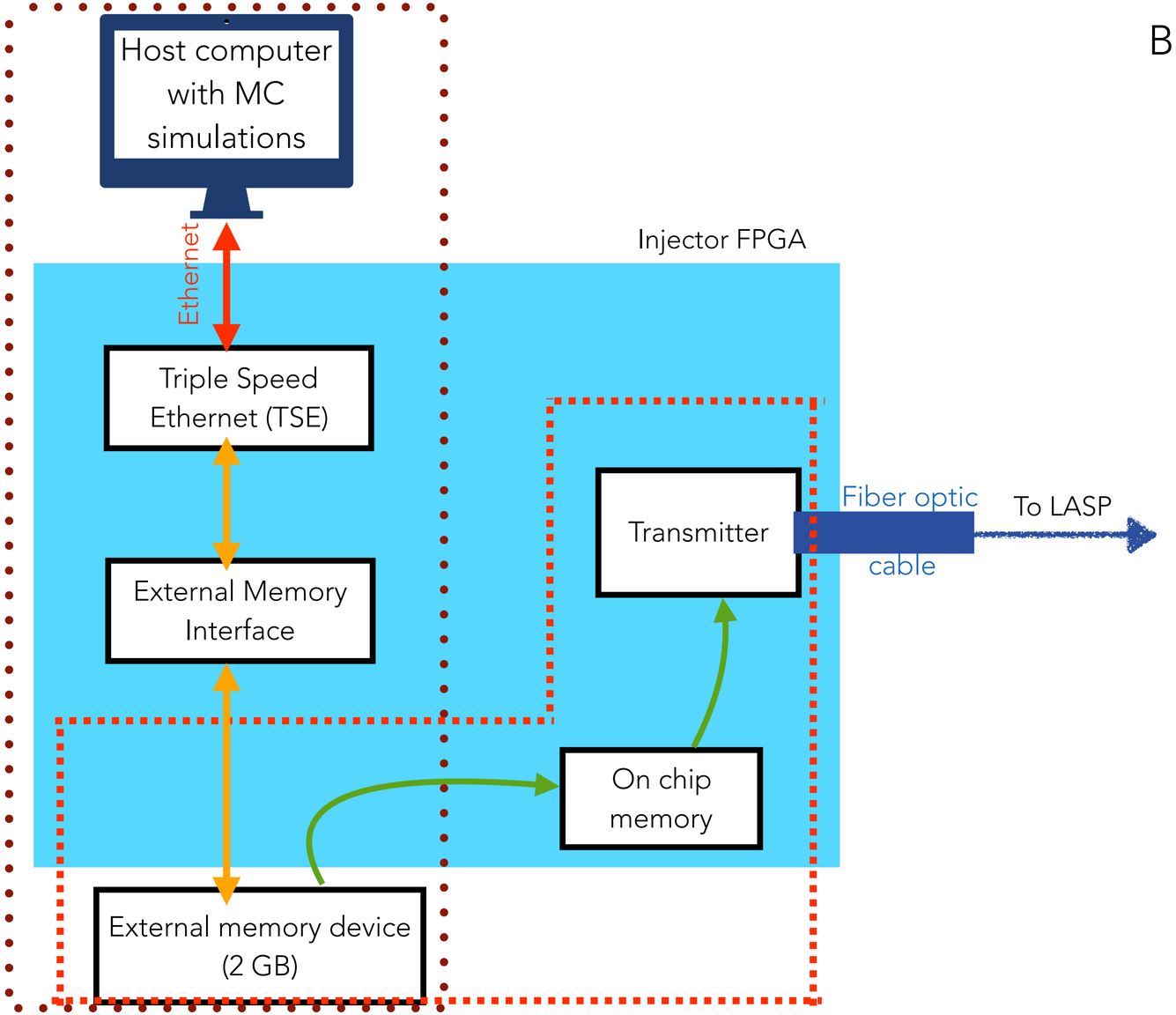


FIG 5: OVERVIEW OF INJECTOR DESIGN

Broken down into two stages:

1. Transfer data from PC into storage via Ethernet using the UDP/IP protocol
2. Retrieval of data from storage. Packaging of data in a format that replicates the FEB2 payload

- ☑ The injector monitors incoming Ethernet frames and strips it down to provide a UDP payload only
- ☑ As a consequence, the Injector “lives” inside an Ethernet network
- ☑ Data sent from the Ethernet is then stored in a 2GB External memory device.
- ☑ Once all 2GB of data is stored, the contents are retrieved, packaged and are sent to the LASP
- ☑ Injection of contents continues until user intervention

ETHERNET DATA TRANSFER

- Using a packet sniffer (e.g. Wireshark), one can intercept and monitor the traffic across a particular network.
- The injector is tested by connecting it to a moderately busy campus network switch. The workstation sending the data is connected to the *same* network switch.
- Dumping of contents received by the injector show that all the ethernet packets are transferred correctly

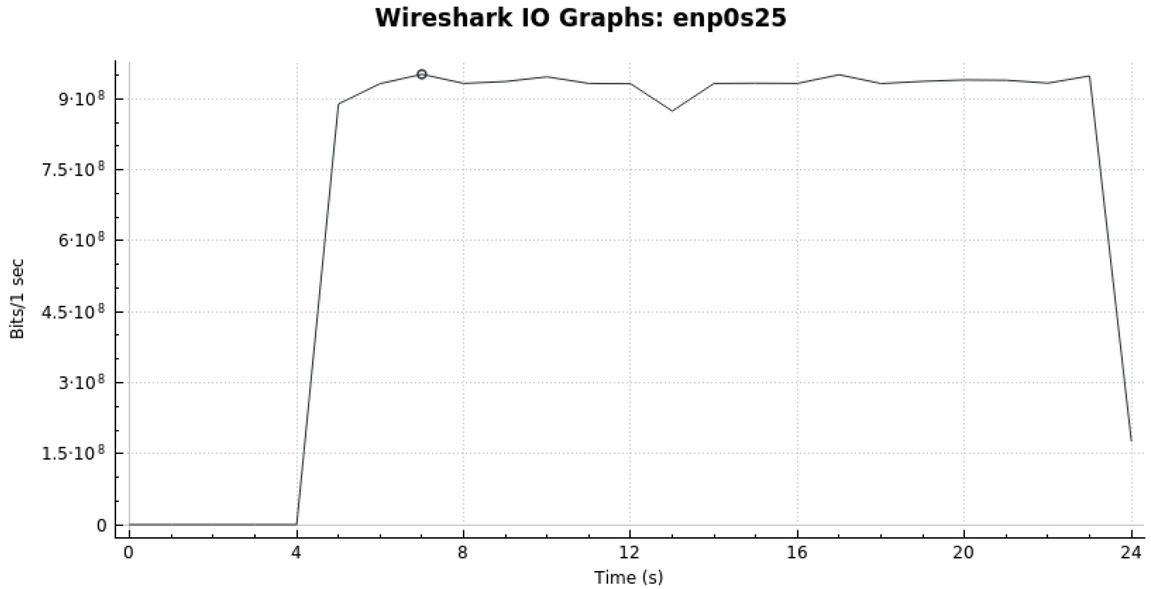


FIG 6: DATA TRANSMISSION SPEED AS MONITORED BY AN ETHERNET PACKET SNIFFER

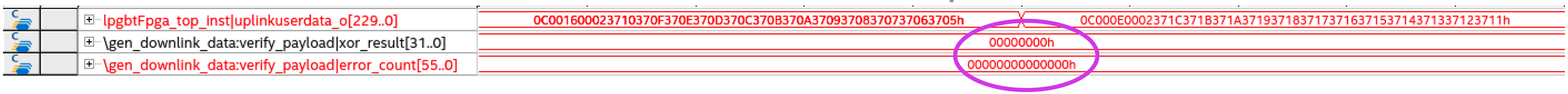
The Ethernet throughput is measured @ ~930Mbps i.e. takes ~18s to send 2GB

This is at the limit of the GbE protocol.

DATA INJECTION TO LASP

- Signals inside the FPGA can be probed and measured - somewhat like an oscilloscope.
- To verify the injection, the signals received by the LASP are monitored and are confirmed to be the same as sent by the injector. Additionally, a simple checksum is sent with every payload and recalculated at the receiving end to verify transmission accuracy
- The incoming signal from the injector as well as the error counter (checksum verification) is probed continuously.

Normal sequence



Transmission accuracy = 100%*

* The checksum will not be able to detect a flipping of an even number of bits.
The FEB2-LASP protocol used has advanced correction features (e.g FEC) which ensures the integrity of data transmission

CONCLUSIONS

- The Injector project is designed and built and is now being used within the LASP firmware community.

SPECIFICATION (SUMMARIZED)

"The data injector shall provide, with the **highest fidelity**, **22 channels** of **FEB2 payloads** transmitted at **10.24 Gbps**. The payload should be **user-controlled** which can help test the LASP for different cases. Data injection should occur for **as long as possible**"

➡ **Highest fidelity:** 100% transmission accuracy

➡ **22 channels**: Only 4 channels implemented (limited by FPGA hardware)

➡ **FEB2 payloads**: 12 ADCs + 2BCIDs are extracted from the memory device …

➡ **10.24 Gbps**: … and are transmitted at the FEB2 speeds …

➡ **User-controlled**: 2 GB of user-defined data

➡ **As long as possible**: for an indefinite period

THANK YOU!

YOUR QUESTIONS/COMMENTS ARE MOST APPRECIATED

SPECIAL MENTION 👏🙏

This work has been made possible by the very gracious help and support of the following people

- My supervisors - **Prof. R. Keeler** and **Prof. R. McPherson**
- **Dr. Sam de Jong** and the **whole LASP Firmware group**

REFERENCES

(1) LHC Underground layout with its experiments, http://te-epc-lpc.web.cern. ch/te-epc-lpc/machines/lhc/pagesources/LHC-Underground-Layout.png. Accessed: Jan 2022

(2) The ATLAS Collaboration. ATLAS Liquid Argon Calorimeter Phase-II Upgrade Technical Design Report, 2018

(3) Intel Corp. Intel Stratix 10 GX FPGA Development Kit User Guide, 2019