DUNE Electronics, DAQ and Trigger

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on behalf of DUNE Collaboration

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Outline

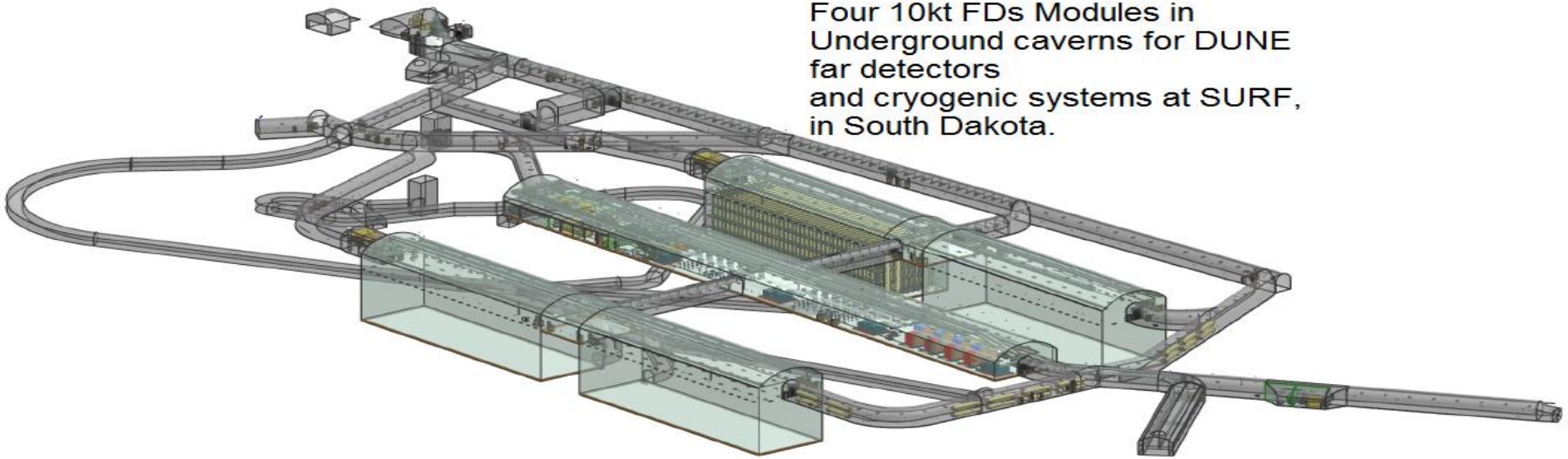
- DUNE Far Detectors: Single Phase and Dual Phase
- TPC readout: Cold electronics ,Warm interface.
- Photon detector electronics
- DAQ Data flow and trigger

DUNE experiment

- DUNE primary physics goals :
  i. Precise measurement of neutrino oscillations parameters using υ_μ and $\bar{\upsilon}_\mu$ beams from Fermilab.
  ii. Detect and measure the υ_e flux from a core-collapse supernova within our galaxy
  iii. Search for proton decay in several important decay modes
- Long-Baseline Neutrino Facility (LBNF), hosted by Fermilab has three major components: 1. Wide band neutrino beam 2. **Near Detector** (ND) Hosted at Fermilab and 3. **Far Detector** (FD) four LArTPC detectors hosted at SURF, 1.5 km depth.

*Create specific requirements on DAQ architecture, in terms of **trigger** and **data buffer** (slide 4)*

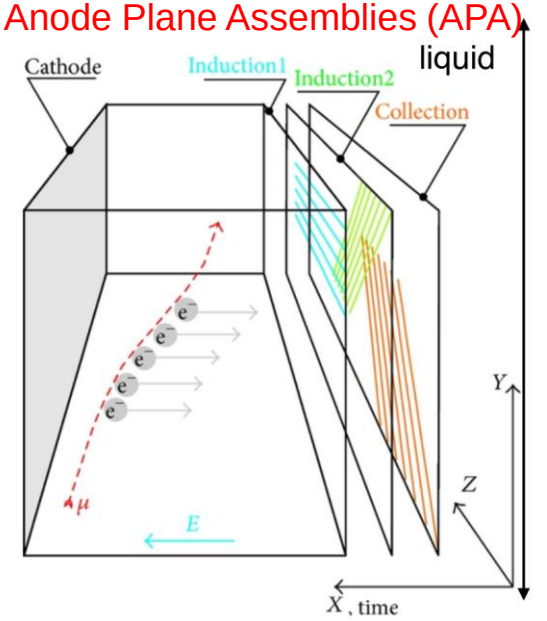
- **In these slides we focus only on Far detector**



Far detector: Single phase and Dual phase

- To achieve the physics goals DUNE is considering two LArTPC technologies:
  - Single-phase (SP): maximum drift length **3.53m** and cathode 180 kV. **No signal amplification in the liquid, so readout requires very low-noise electronics**.
  - Dual-phase (DP): Ionization charges transferred into the gas above the liquid and **amplified** in the gas phase using large electron multipliers (**LEMs**). **Reduces the requirements on the electronics**, **longer drift**, and higher voltage cathode 600 kV. The maximum drift length is 12m. **Less channels per module**.

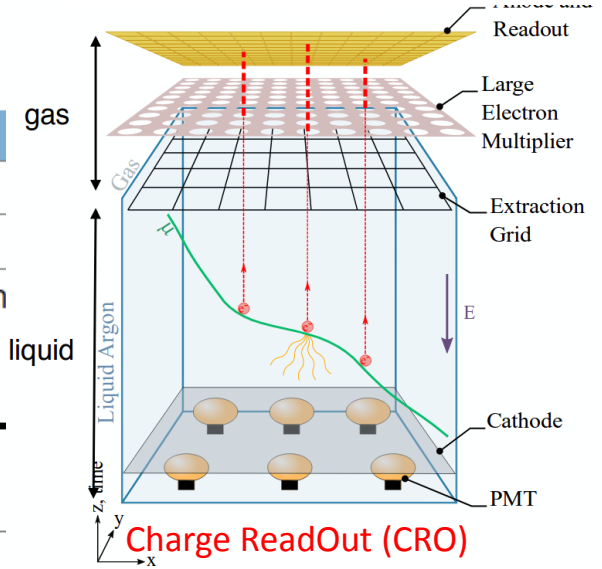
Anode Plane Assemblies (APA)



- Here is the comparative detectors electronics specifications:

Parameter	single-phase	dual-phase
TPC unit	APA	CRO crate
Unit multiplicity	150	240
Channels per unit	2560 (**960** collection)	**640** (all collection
ADC sampling	2 MHz	2.5 MHz
ADC resolution	12 bit	12 bit
Aggregate from CE	1440 GB/s	576 GB/s
Aggregate with compression	288 GB/s (5×)	58 GB/s (10×)

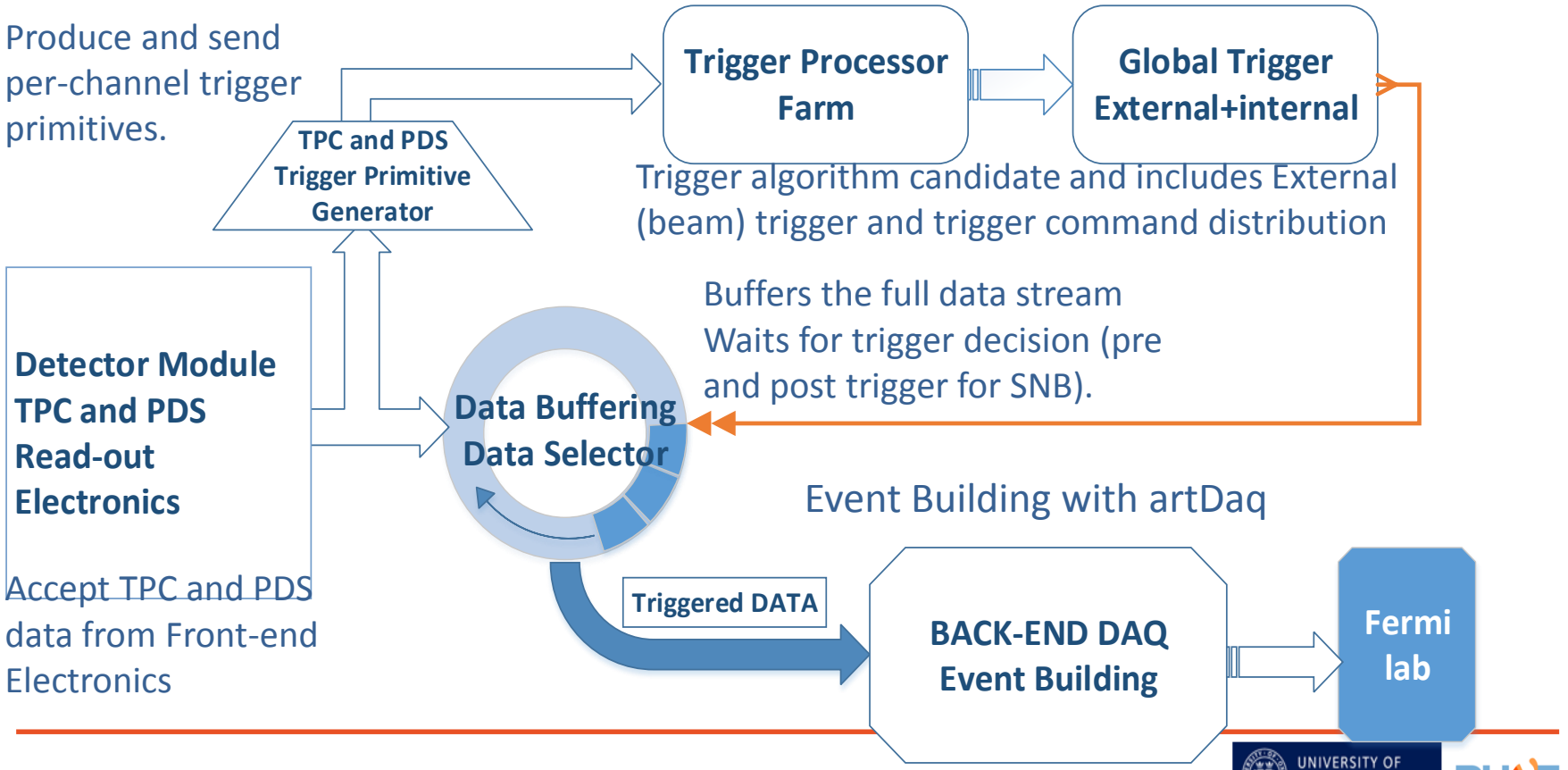
pre-trigger data rate of FECs and no compression



Charge ReadOut (CRO)

DUNE DAQ and trigger high level design simplified

- We need a self triggering detector for proton decays, atmospheric neutrinos and supernova-burst (SNB) neutrinos.
- The SNB physics information is contained in a time window that is tens of seconds long
- **High level** design of DAQ addresses DUNE physics programs, including trigger processing system and data buffering (data rate in backup slides)



SP- TPC front end readout

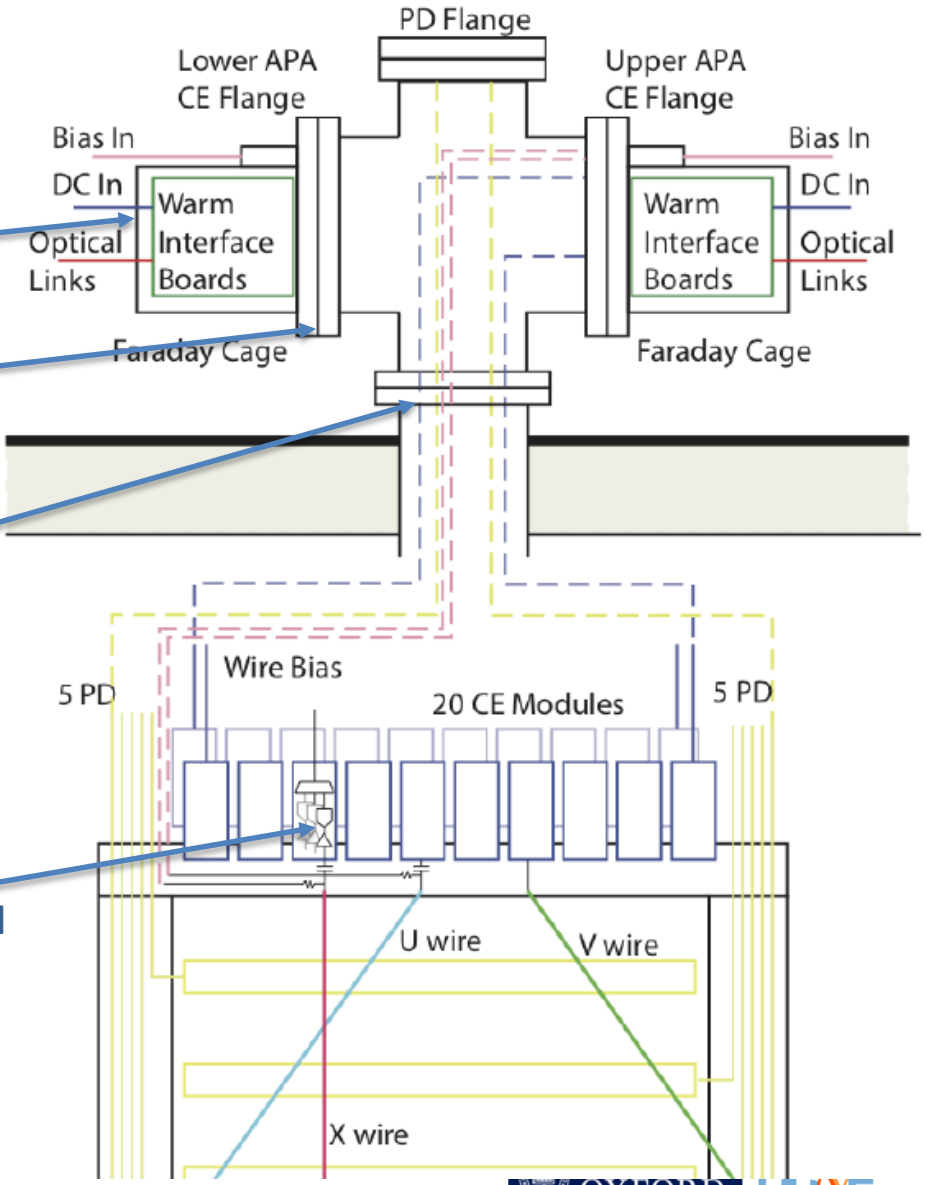
TPC electronics can be classified roughly in three categories: Warm electronics (or interface), Cold flange + Signal feed-through and Cold electronics.

1- Warm interface electronics crates (WIECs)
- Mounted on the signal flanges
- Warm interface boards (WIBs)
- Power and timing cards (PTCs)

2a- CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection

2b- Signal feed-through
CE feedthrough to pass the data, clock and control signals, LV power and APA wire-bias voltages

3- Front End Motherboard
(FEMB) 128 channels of digitized wire readout enclosed in CE Box



SP - TPC readout FEMB

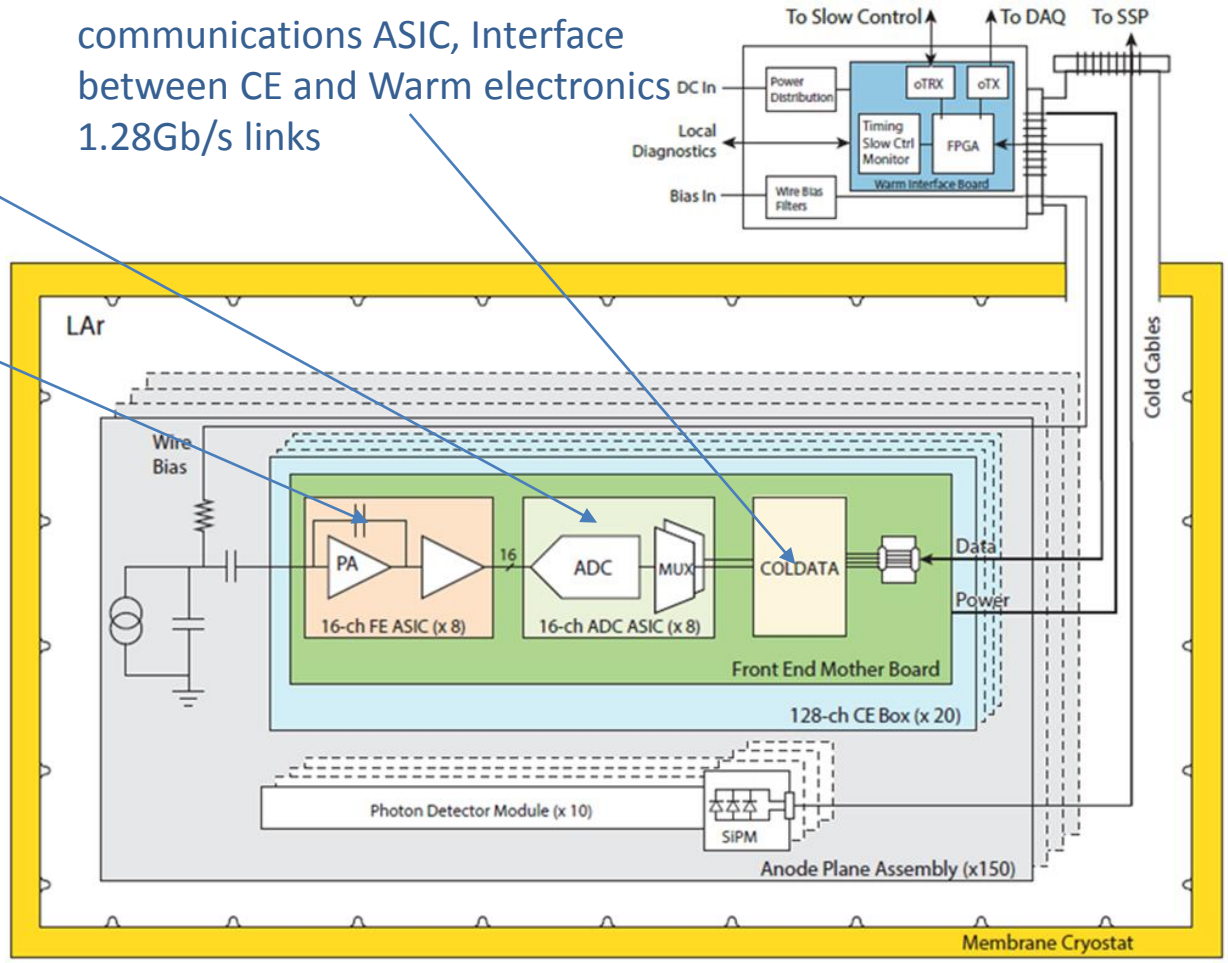
- Front-End Mother Board (**FEMB**) includes three types of ASICs: (More details are in backup slides)

ColdADC
16-channel 12-bit ADC ASIC operating at **2 Msps**, **pipelined ADCs** operating at 16 MHz. Highly configurable via UART or I2C

COLDATA
64-channel control and communications ASIC, Interface between CE and Warm electronics 1.28Gb/s links

LArASIC
16-channel ASIC for amplification and pulse shaping, **Gain** 4.7 to 25mV/fC, **Peaking** time 0.5, 1, 2, 3 µs

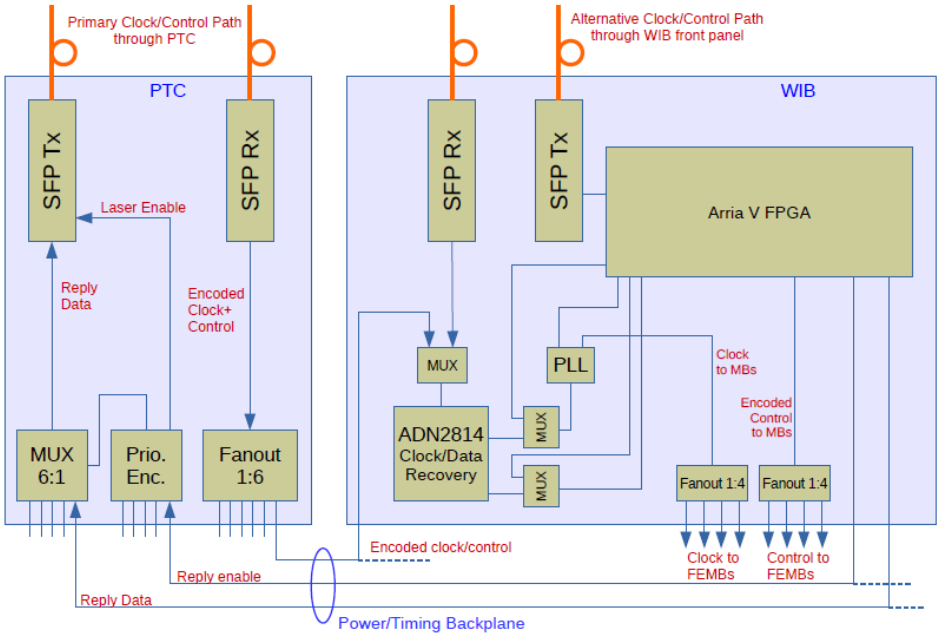
FEMB
Receives signals from **40 U** wires, **40 V** wires, and **48 X** wires

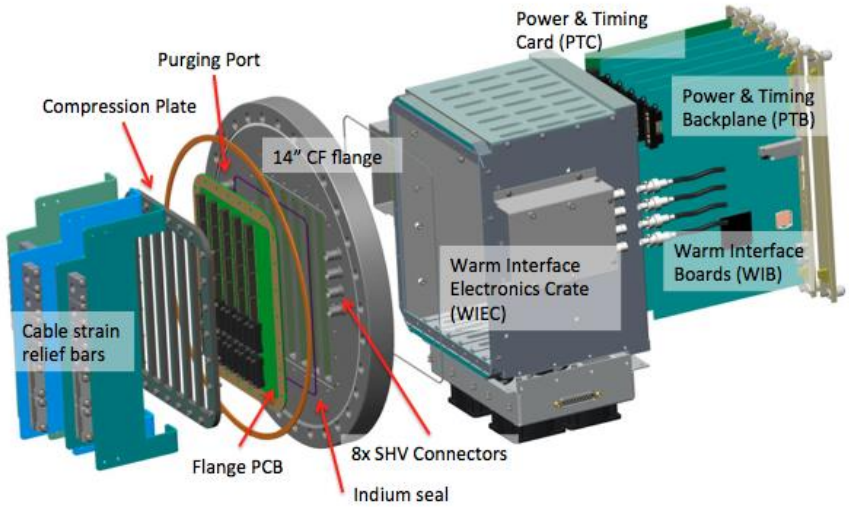


SP - TPC readout Warm Interface Electronics

- The warm interface electronics (WIB) provide an interface between the CE, DAQ, timing, and slow control systems, including local power control at the flange and a real-time diagnostic readout.
- WIBs are housed in the warm interface electronics crate (WIEC) attached directly to the CE flange.
- The WIEC shown in bottom right contains one power and timing card (PTC), five warm interface boards (WIBs) and a passive power and timing backplane (PTB)

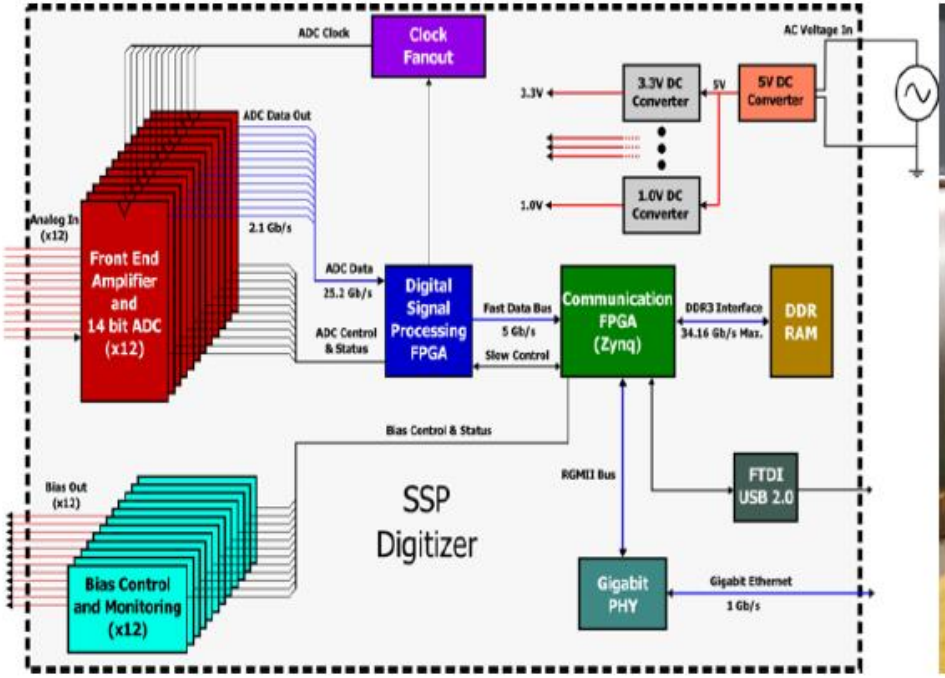
Developed for ProtoDUNE-DP





SP – Photon Detection System readout

- SiPM Signal Processor (SSP) are developed for ProtoDUNE-SP. It contains 12 readout channels packaged in a 1U module. (shown in bottom right)
- The unamplified analog signals from the SiPMs are transmitted to outside the cryostat over a 25m cable. A 14-bit, 150-MSPS ADC digitizes the SiPM signal waveforms.
- Separate 12-bit high-voltage DAC to provide bias to each SiPM.
- Triggered by a beam event, or to provide header information when self-triggered
- 1 Gb/s Ethernet send the waveform through full TCP/IP *Check Zelimir talk*

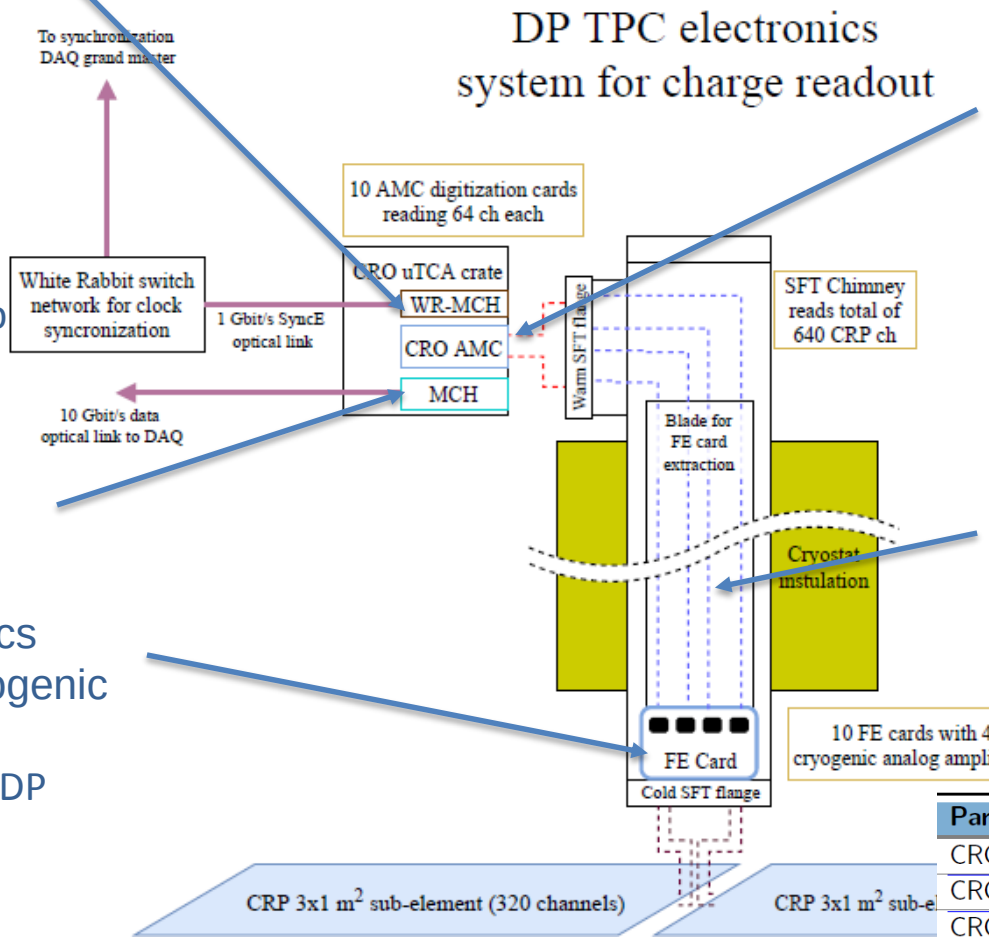


DP - TPC readout, charge readout (CRO)

White Rabbit µTCA Carrier Hub (WR-MCH) for AMC clock synchronization

MicroTCA Carrier Hub (MCH) streams the data from AMCs via a dedicated optical link

Front-end (FE) Analog electronics operating at cryogenic temperatures
Accessible during DP under operation, through SFT



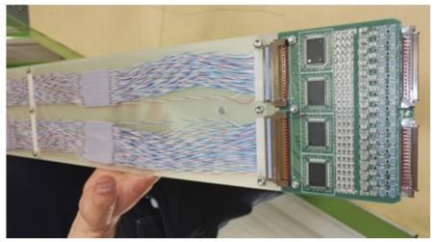
Advanced mezzanine cards (AMCs) Holds digitizing electronics

signal feedthrough chimneys (SFT chimneys) 2.3m long.

Parameter	Value
CRO channels	153,600
CRO continuous sampling rate	2.5 MHz
CRO ADC resolution	12 bit
CRO data compression factor	10
CRO data flow	430 Gibit/s

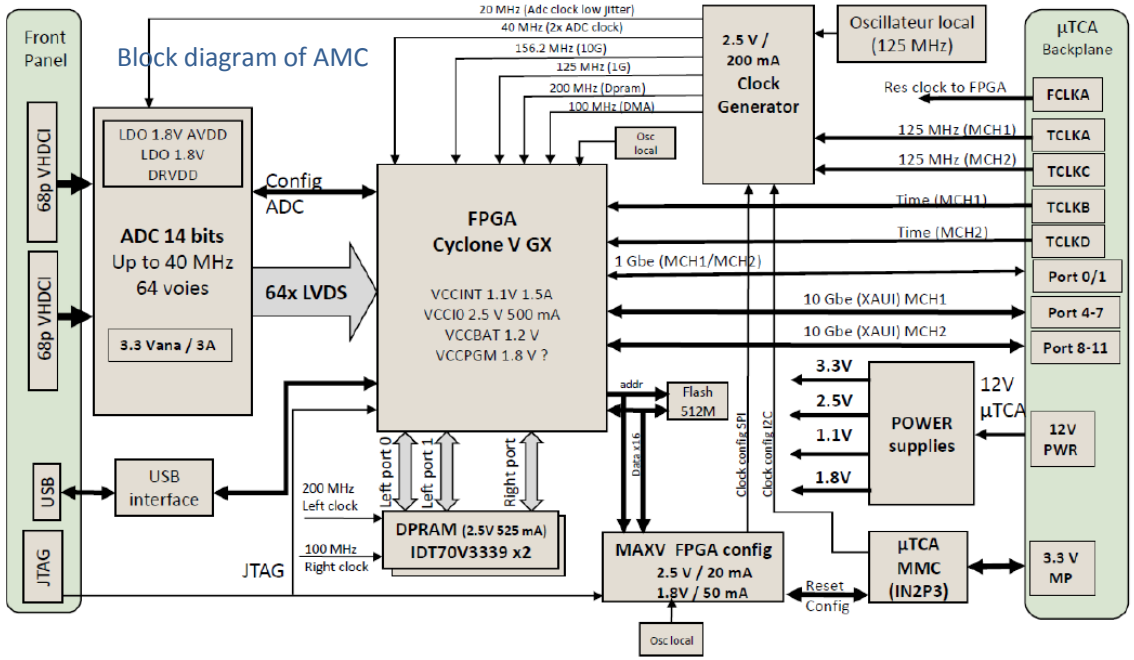
DP - TPC readout, Analog Front-end

- **Cryogenic Analog Front-end Electronics**
  - ASIC CMOS 0.35 µm technology
  - Each ASIC contains 16 amplifier channels with differential line buffers
  - Average value of the noise RMS is around 1.7 ADC
- **Digital Advanced Mezzanine Card Electronics**
  - Digitize the data from the FE amplifiers and transmit them to the DAQ system.
  - Include a final stage of analog shaping before the ADC input
  - Each card has eight ADC chips (AD92574), 2 dual-port memories, and an PGA Altera6 Cyclone V
  - 2.5MSPS 12 bit

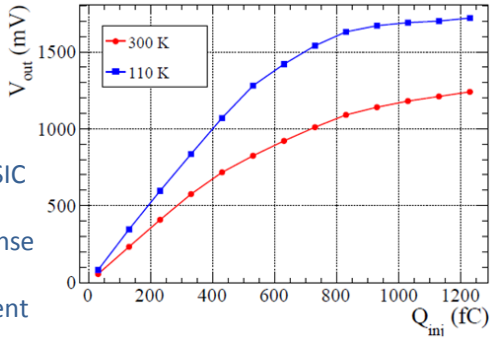


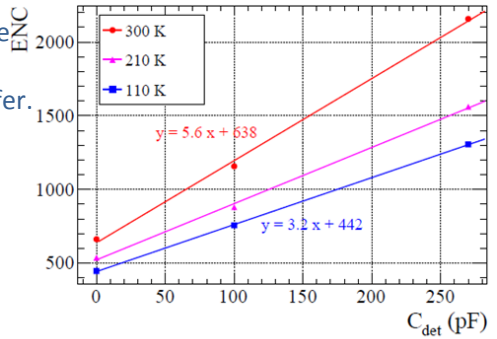
Analog cryogenic FE card mounted on the extraction blade, which is a part of the SFT chimney sub-system.

Block diagram of AMC



Cryogenic FE ASIC properties: amplifier response (top) and noise (right) at different temperatures measured at the output of differential buffer.





DP - TPC Light Readout 1

- **Light readout (LRO)**
  - Collects and digitizes the signals from the PDS, Diagram very similar to CRO
  - The LRO card is a 16 channel AMC containing one16 channel 14 bit 65MHz ADC (AD9249) and one CATIROC ASIC.
- The analog signals from each PMT channel are split equally into two separate branches
  - One path (waveform branch), through an anti-aliasing low-pass filter and the 14 bit 65MHz ADC (AD9249), produces continuous digitization of the PMT waveform data, which are down-sampled to 2.5MHz prior to the transmission to DAQ.
  - The other (CATIROC branch) is routed directly to the CATIROC ASIC for precise measurements of pulse charge and timing. Both paths produce data continuously and independently

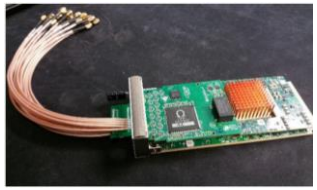
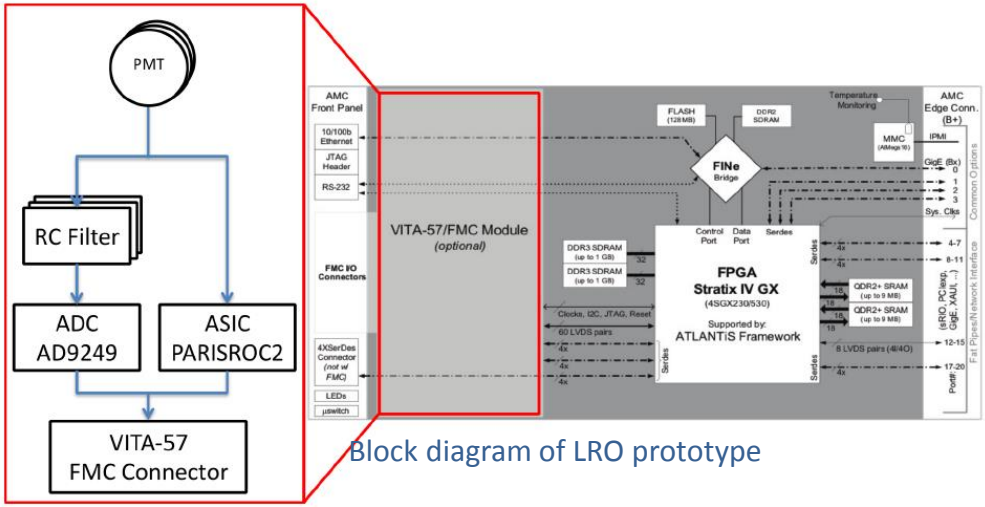
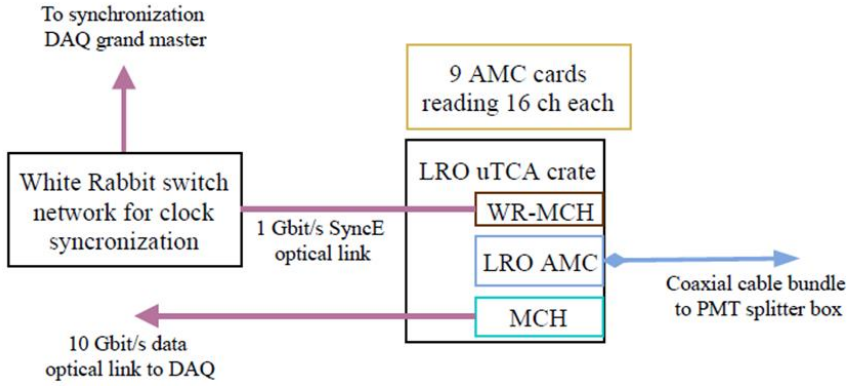


Photo of the LRO prototype.

Parameter	Value
LRO channels	720
LRO continuous sampling rate	2.5 MHz
LRO ADC resolution	14 bit
LRO data compression factor	1
LRO data flow	24 Gibit/s

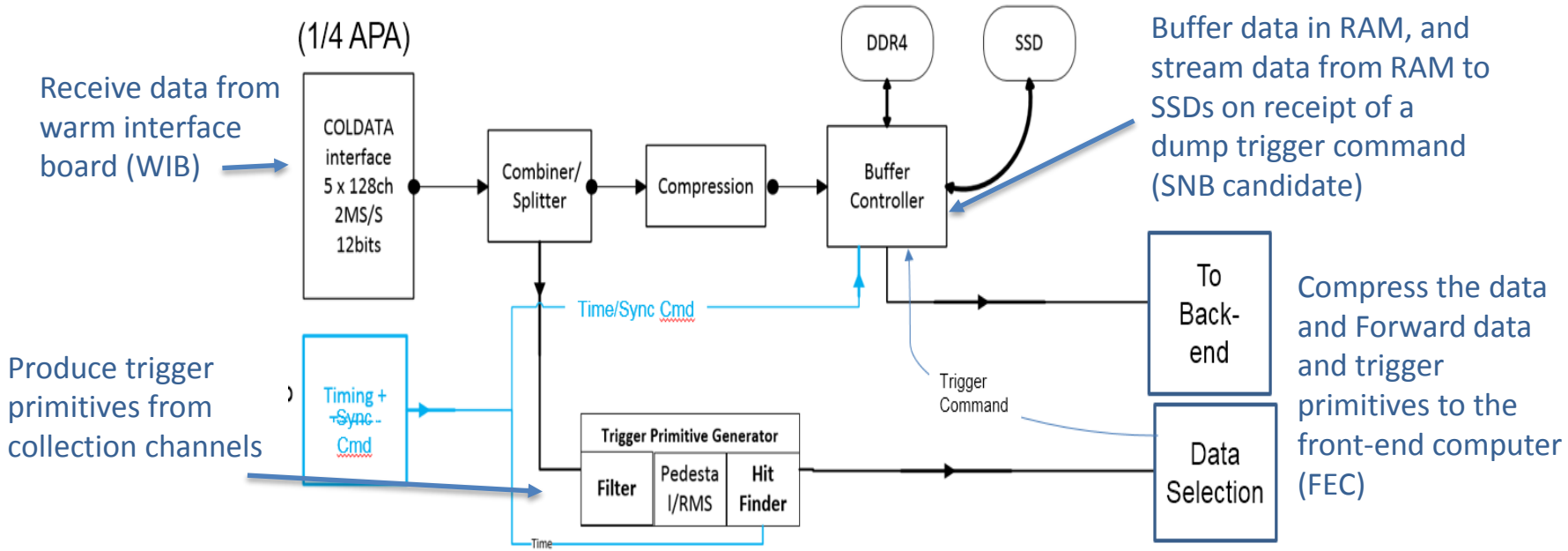


Block diagram of LRO prototype



SP - Front-end Readout and Buffering (FER)

- The DP and SP have different FE readout technology, data throughout and format, we need a unified interface to DUNE offline computing.
- Currently, two major variations for the DUNE DAQ are under consideration. The goal is to reduce this to a single high-level design which will service both SP and DP detector modules.
- The first design, *nominal*, and second design shown next slides in a high-level way in terms of its FER and data and trigger flow. The two variants differ largely at their FEs in terms of the order in which they buffer the data received from FE electronics and use it to form trigger primitives.
- Before showing them let's have a bit more detail about REF shown in below diagram;



SP - Front-end Readout and Buffering

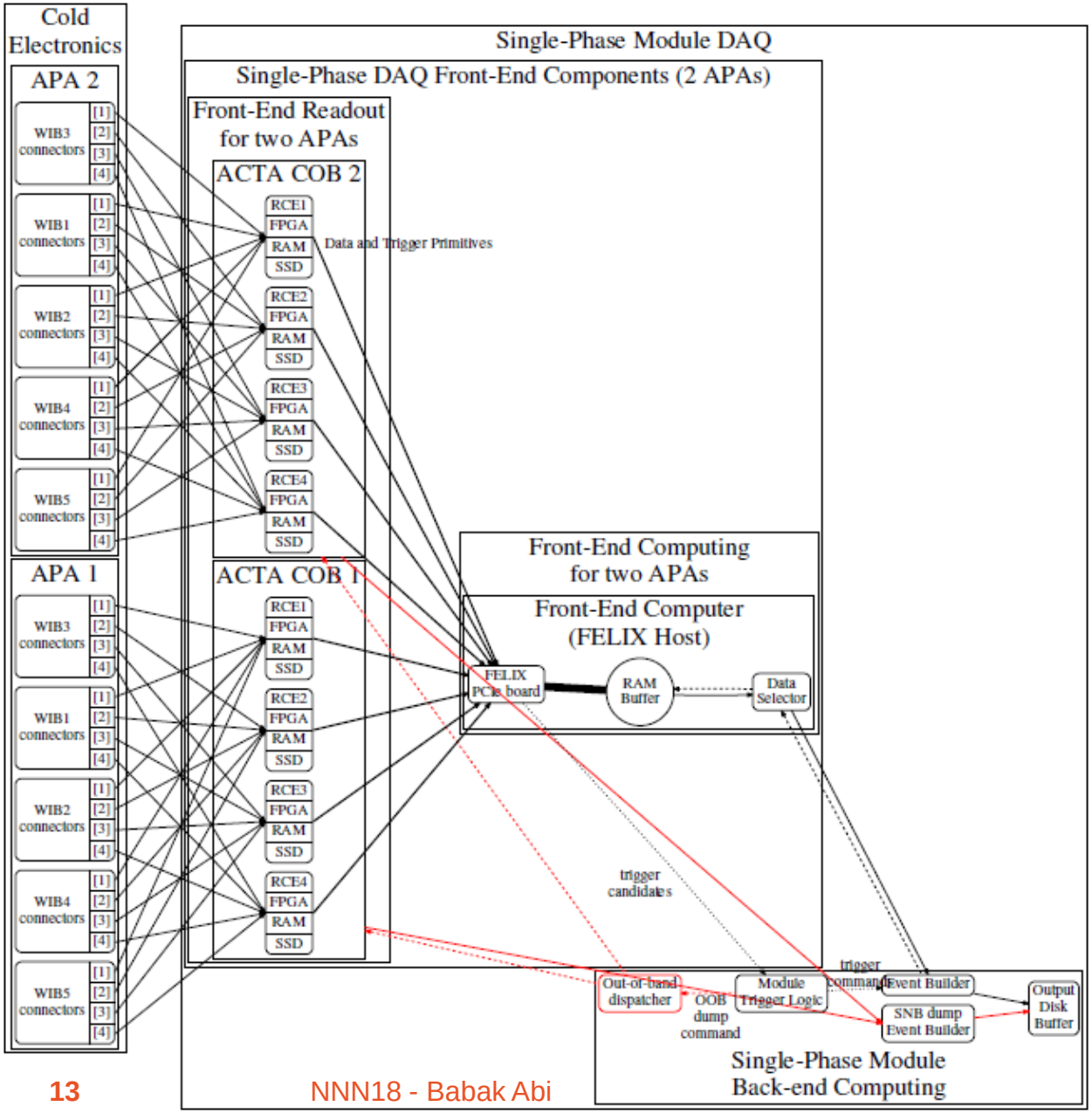
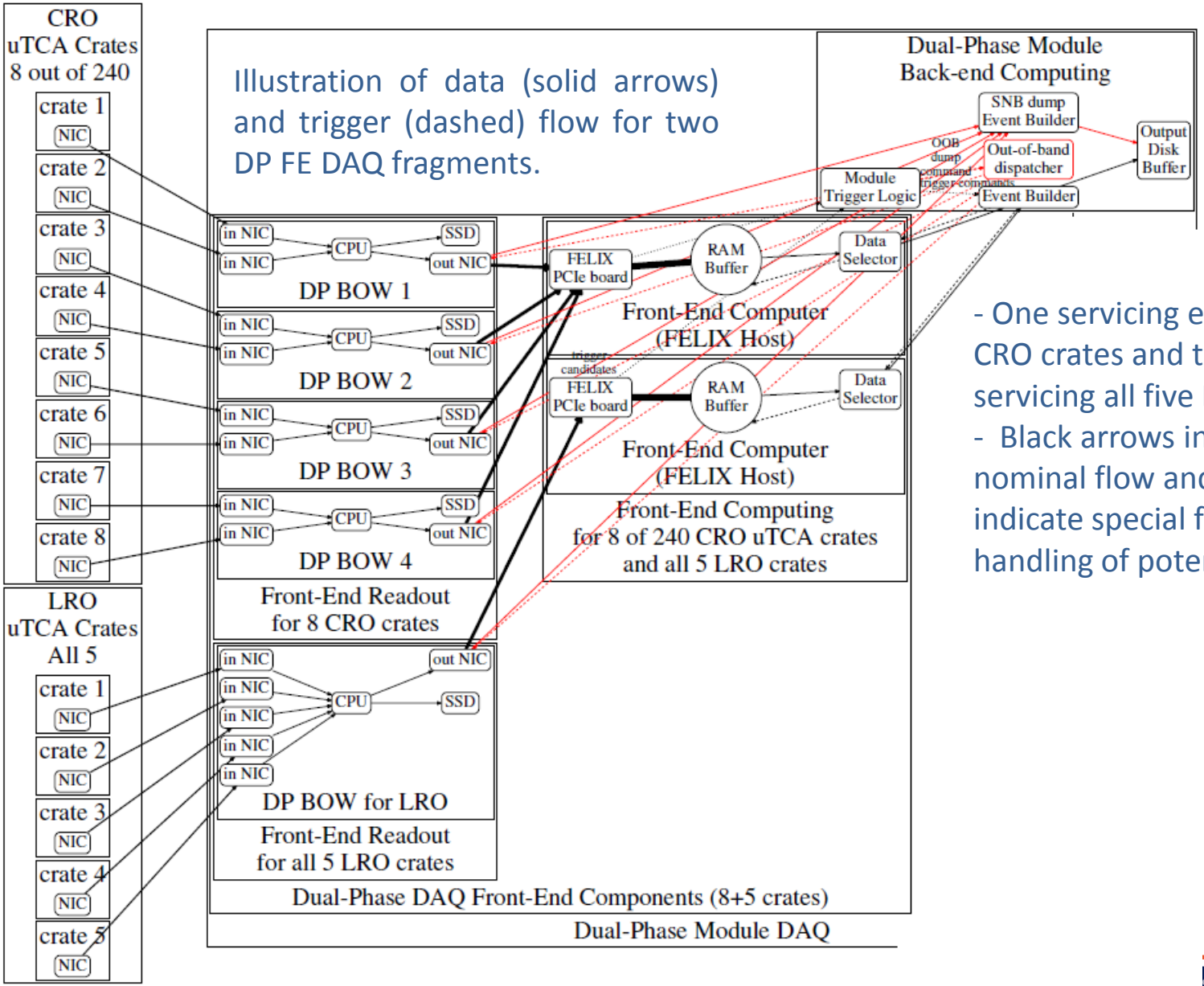


Illustration of data (solid arrows) and trigger (dashed) flow for one SP DAQ fragment (two APAs) in the nominal design.

Black arrows indicate normal data and trigger flow and red indicate special flow for handling of a potential SNB.

DP - Front-end Readout and Buffering

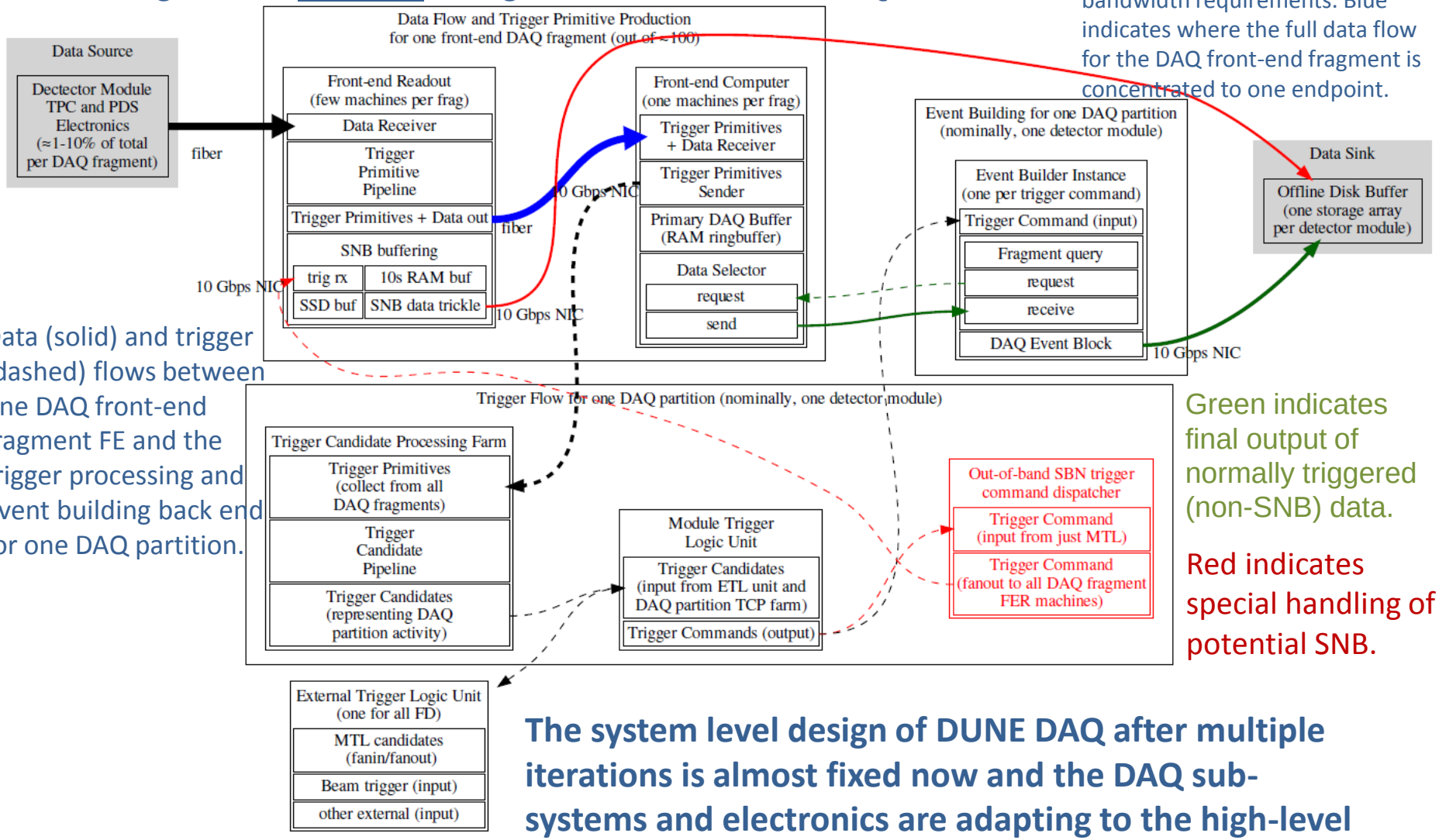


- One servicing eight of 240 CRO crates and the other servicing all five LRO crates.
- Black arrows indicate nominal flow and red indicate special flow for handling of potential SNB.

DAQ Dataflow, Trigger and Event Builder

The high-level, nominal design for the DUNE FD DAQ

Line thickness indicates relative bandwidth requirements. Blue indicates where the full data flow for the DAQ front-end fragment is concentrated to one endpoint.



Data (solid) and trigger (dashed) flows between one DAQ front-end fragment FE and the trigger processing and event building back end for one DAQ partition.

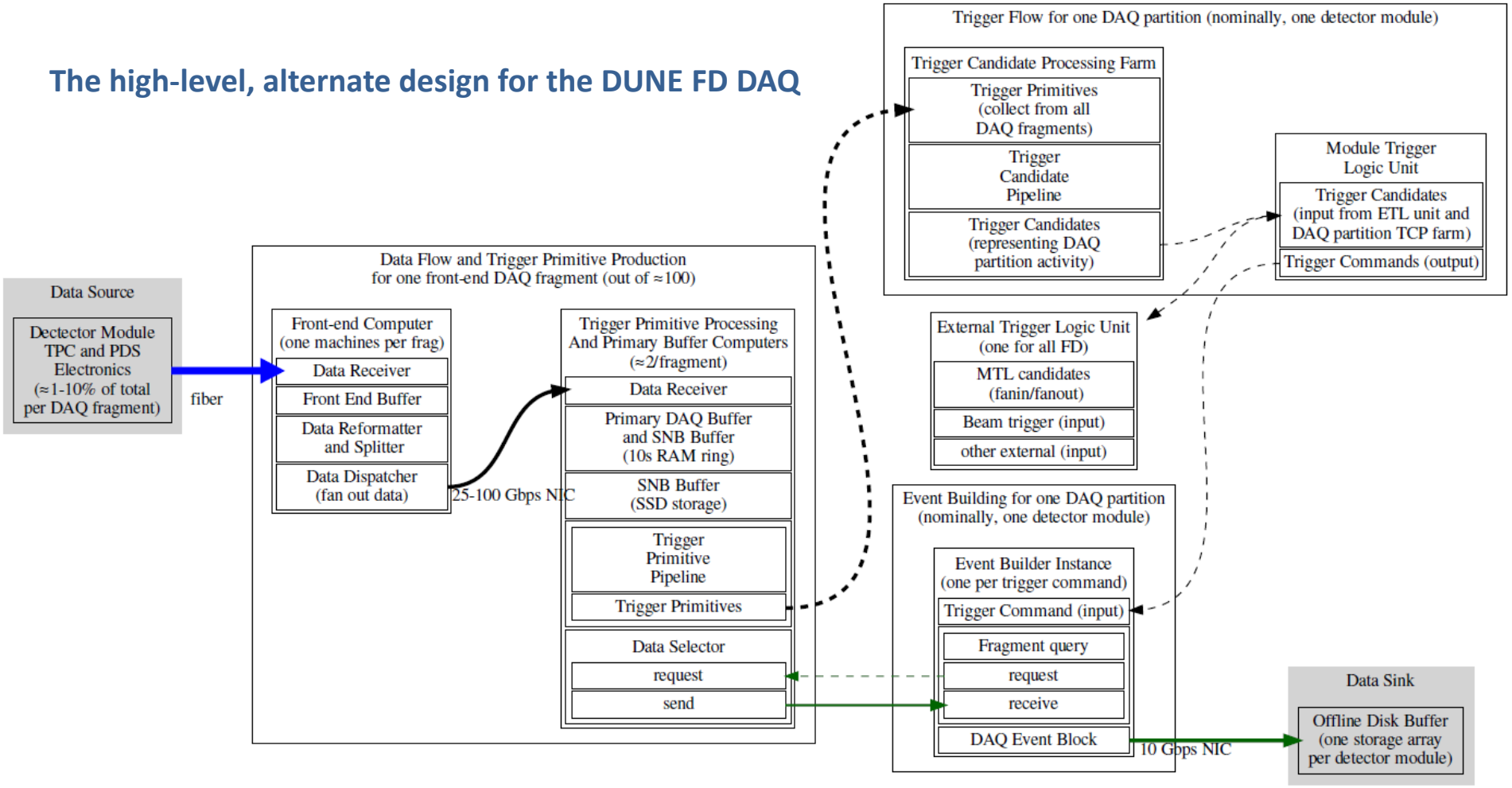
Green indicates final output of normally triggered (non-SNB) data.

Red indicates special handling of potential SNB.

The system level design of DUNE DAQ after multiple iterations is almost fixed now and the DAQ sub-systems and electronics are adapting to the high-level data flow design.

DAQ Dataflow, Trigger and Event Builder

The high-level, alternate design for the DUNE FD DAQ



Conclusion

- There are several large and interesting challenges in the DUNE DAQ design, including the large data rate and volume, the long readout-window for SNB, and the internally generated triggers. The challenges have been met and have resulted in a solid design..
- Many of the analogue and digital electronics in DUNE TPC readout are based on components that have been demonstrated in LArTPC detectors e.g. ICARUS, MicroBooNE, ProtoDUNE.
- The back end DAQ electronics utilises both industry-standard modules and custom systems. It allows considerable programmable flexibility in combining FPGA and CPU features.
- The ProtoDUNE DP and SP detectors are crucial for establishing DUNE technology and we studying their performance to refine the DUNE DAQ.
- The system level design of DUNE DAQ after several iterations is almost fixed now and the DAQ sub-systems and electronics are adapting to the high-level data flow design.

Back Up Slides

DUNE Data rates

- Anticipated annual, uncompressed data rates for a single SP module. The rates for normal (non-SNB triggers) assume a readout window of 5.4 ms. For planning purposes these rates are assumed to apply to a DP module as well, which has a longer readout time but fewer channels. In reality, application of lossless compression is expected to provide as much as a 5× reduction in data volume for the SP module and as much as 10× for the DP module.

Event Type	Data Volume PB/year	Assumptions
Beam interactions	0.03	800 beam and 800 dirt muons; 10 MeV threshold in coincidence with beam time; include cosmics
Cosmics and atmospherics	10	10 MeV threshold, anti-coincident with beam time
Front-end calibration	0.2	Four calibration runs per year, 100 measurements per point
Radioactive source calibration	0.1	Source rate $\leq$10 Hz; single fragment readout; lossless readout
Laser calibration	0.2	1×10^6 total laser pulses, lossy readout
Supernova candidates	0.5	30 seconds full readout, average once per month
Random triggers	0.06	45 per day
Trigger primitives	$\leq$6	All three wire planes; 12 bits per primitive word; 4 primitive quantities; ^{39}Ar-dominated

SP - TPC readout FEMB

- TPC electronics components and quantities for a single APA of the DUNE SP module.

Element	Quantity	Channels per element
Front-end mother board (FEMB)	20 per APA	128
FE ASIC chip	8 per FEMB	16
ADC ASIC chip	8 per FEMB	16
COLDATA ASIC chip	2 per FEMB	64
Cold cable bundle	1 per FEMB	128
Signal flange	1 per APA	2560
CE feedthrough	1 per APA	2560
Warm interface board (WIB)	5 per APA	512
Warm interface electronics crate (WIEC)	1 per APA	2560
Power and timing card (PTC)	1 per APA	2560
Power and timing backplane (PTB)	1 per APA	2560

ProtoDUNE SP TPC Front-end DAQ

- ProtoDUNE is running two systems, Reconfigurable Computing Elements (RCE) designed at SLAC for a wide range of applications and Front-End-Link-Exchange (FELIX) that was originally designed for ATLAS;
  - **RCE :** Based on system-on-chip FPGA (Xilinx Zynq) with ARM processor + 1 GB DRAM handles 256 ch. Up to 8 RCEs in cluster-on-board motherboard in AdvancedTCA shelf. 10 Gbps Ethernet for connection between RCE and to DAQ server. Specific board (Rear Transition Module) for receiving optical link from Warm Interface Board.
  - **FELIX** The FELIX is a PCIe card receiving data on point-to-point links from the detector electronics and routing those through a switched network to computers. e.g. ProtoDUNE-SP, data from five WIBs (20 FEBs) are read out over ten 9.6Gbps links into two FELIX cards. Similar to the RCE-based readout, the FELIX generates artDAQ fragments to be sent to the event builder.
- Intensive R&D in various back-end DAQ electronics are planned in parallel to demonstrate of both these systems in ProtoDUNE-SP.
- The final goal is to merge as much as possible to a single technology that could accommodate data coming from both frontend electronics of single phase and dual phase detectors.

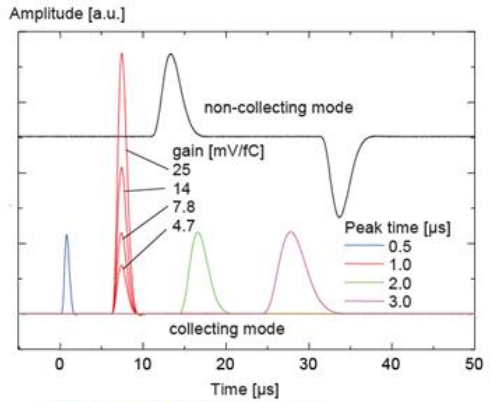
SP - TPC readout FEMB

- Presenting only the baseline FEMB and ASICs, There is one official alternative design, the SLAC nEXO three-chip CRYO ASIC, and one fallback ATLAS-style ADC ASIC.
- Front-End Mother Board (**FEMB**) includes three major parts:

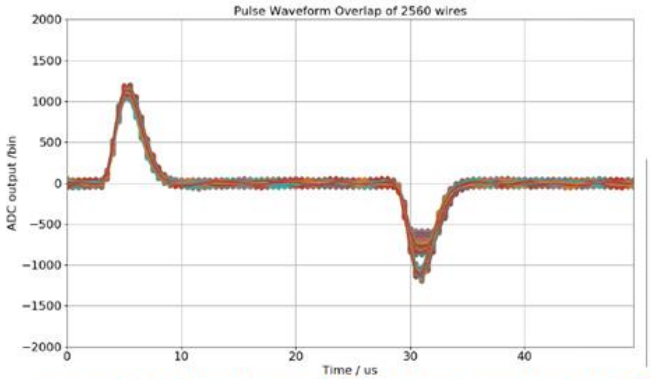
1. Preamplifiers + shaping circuit

- LArASIC :16-channel front-end ASIC, signal amplification and pulse shaping.

The LArASIC receives signals from the CR board :
- charge amplifier circuit with a programmable gain selectable from one of 4.7, 7.8, 14 or 25mV/fC (corresponding to full-scale charge of 300, 180, 100 and 55 fC),
- shaping a high-order anti-aliasing filter with programmable time constant (semi-Gaussian with peaking time 0.5, 1, 2, and 3 µs),
- option to enable AC coupling, and a baseline adjustment for operation with either the collecting (200mV nominal) or the non-collecting (900mV nominal) wires.



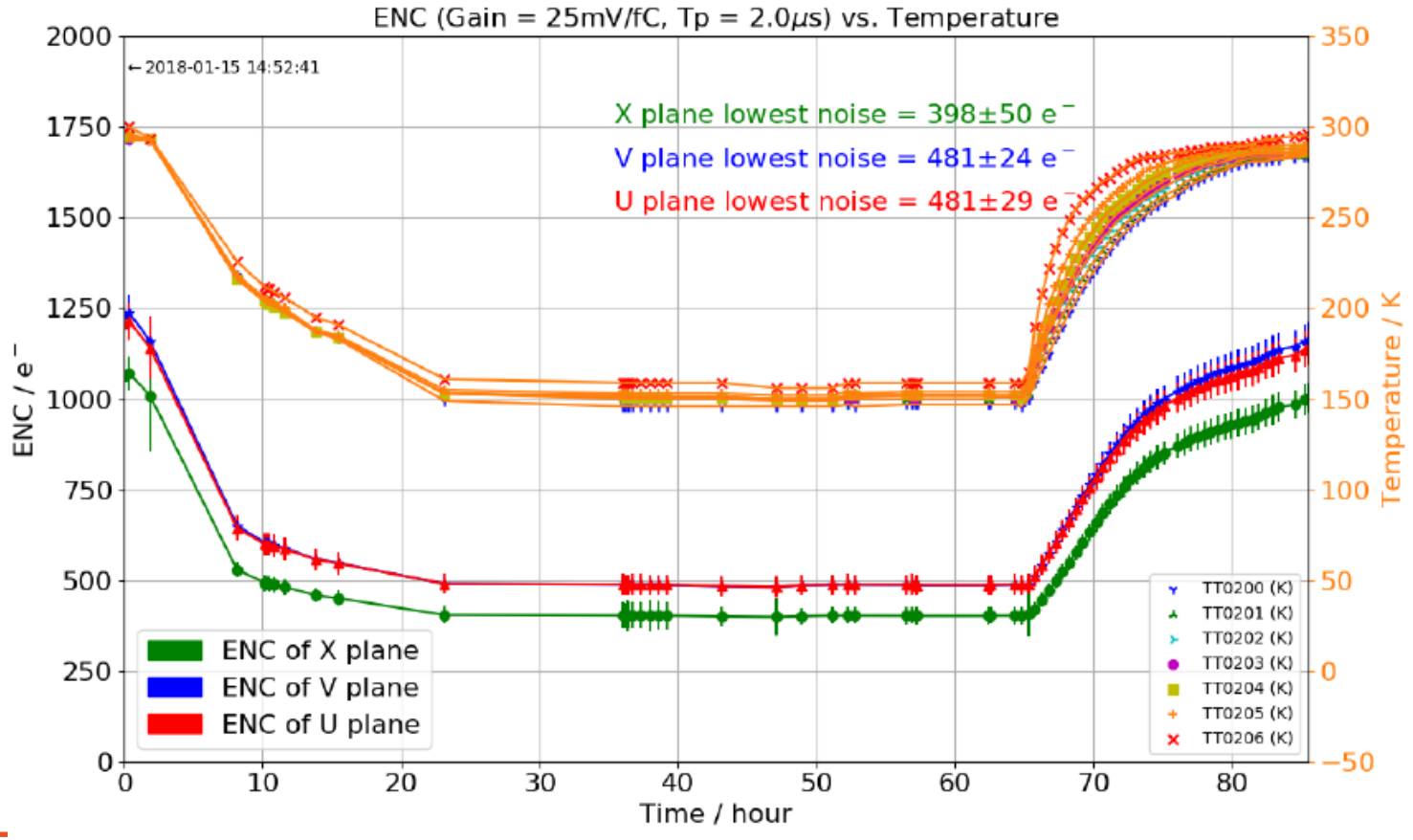
Simulated FE response



measured calibration pulse response overlays for 2560 electronics channels attached to a ProtoDUNE-SP APA

FEMB noise and performance

- ENC in electrons (left axis) for the wrapped induction wires (red and blue curves) and straight collection wires (green curve) as well as the temperature in degrees Kelvin (right axis) for the temperature sensors in the CERN cold box (orange curves) as a function of cold cycle time in gaseous nitrogen for ProtoDUNE-SP APA2. At the lowest temperature of 160 K, the wrapped wires measured 480 e− noise and the straight wires 400 e−. This noise level is consistent with all other ProtoDUNE-SP anode plane assemblies tested in the cold box.



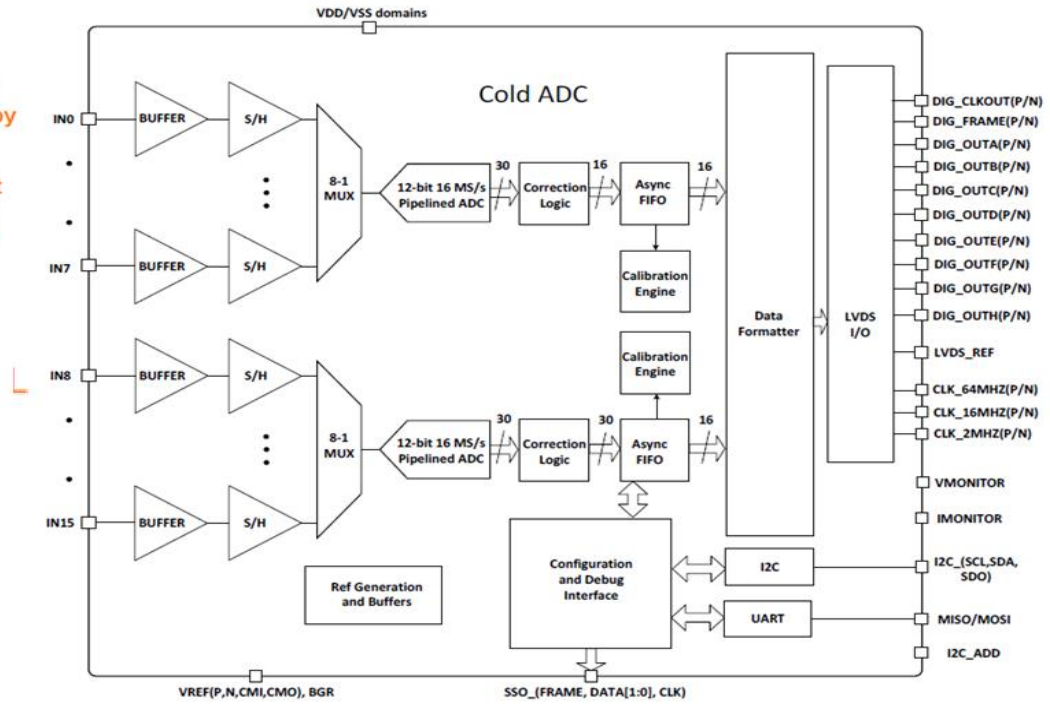
SP - TPC readout FEMB

- Front-End Mother Board (**FEMB**) includes three major parts:
  1. Preamplifiers + shaping circuit
     - LArASIC :16-channel front-end ASIC, signal amplification and pulse shaping.
  2. Cold ADC
     - 16(2x8)channel 12-bit 16 MS/s Pipelined ADC

Cold ADC, block diagram

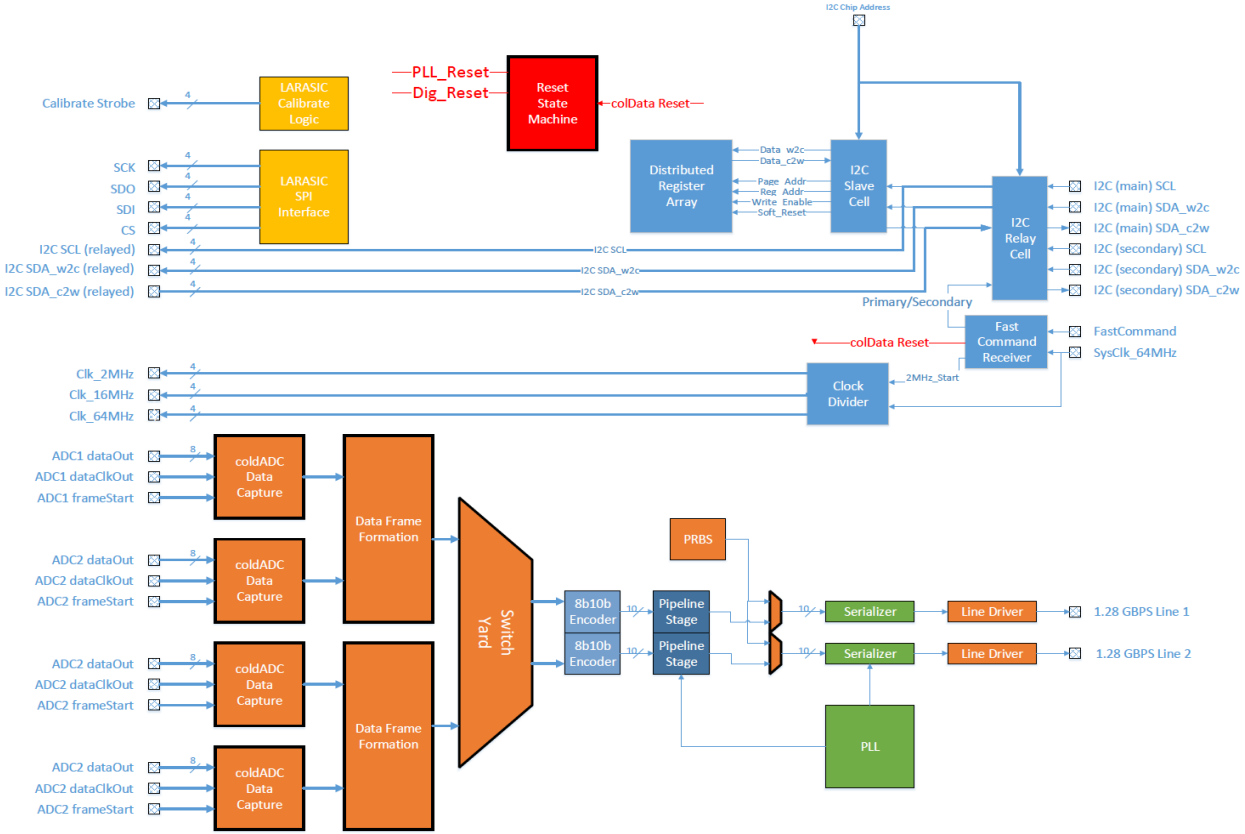
The analog samples are multiplexed by 65nm CMOS technology.

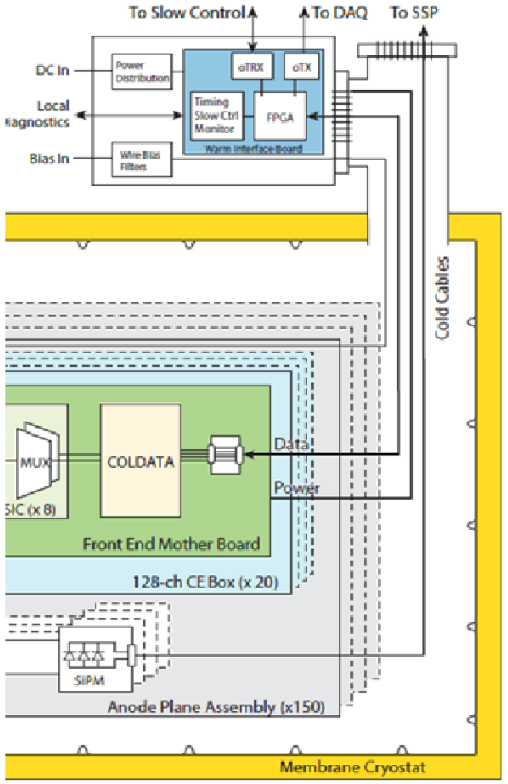
eight and digitized by calibrated 12 bit pipelined ADCs operating at 16 MHz.



collaboration of scientists and engineers at BNL, Fermilab, and LBNI

SP - TPC readout FEMB



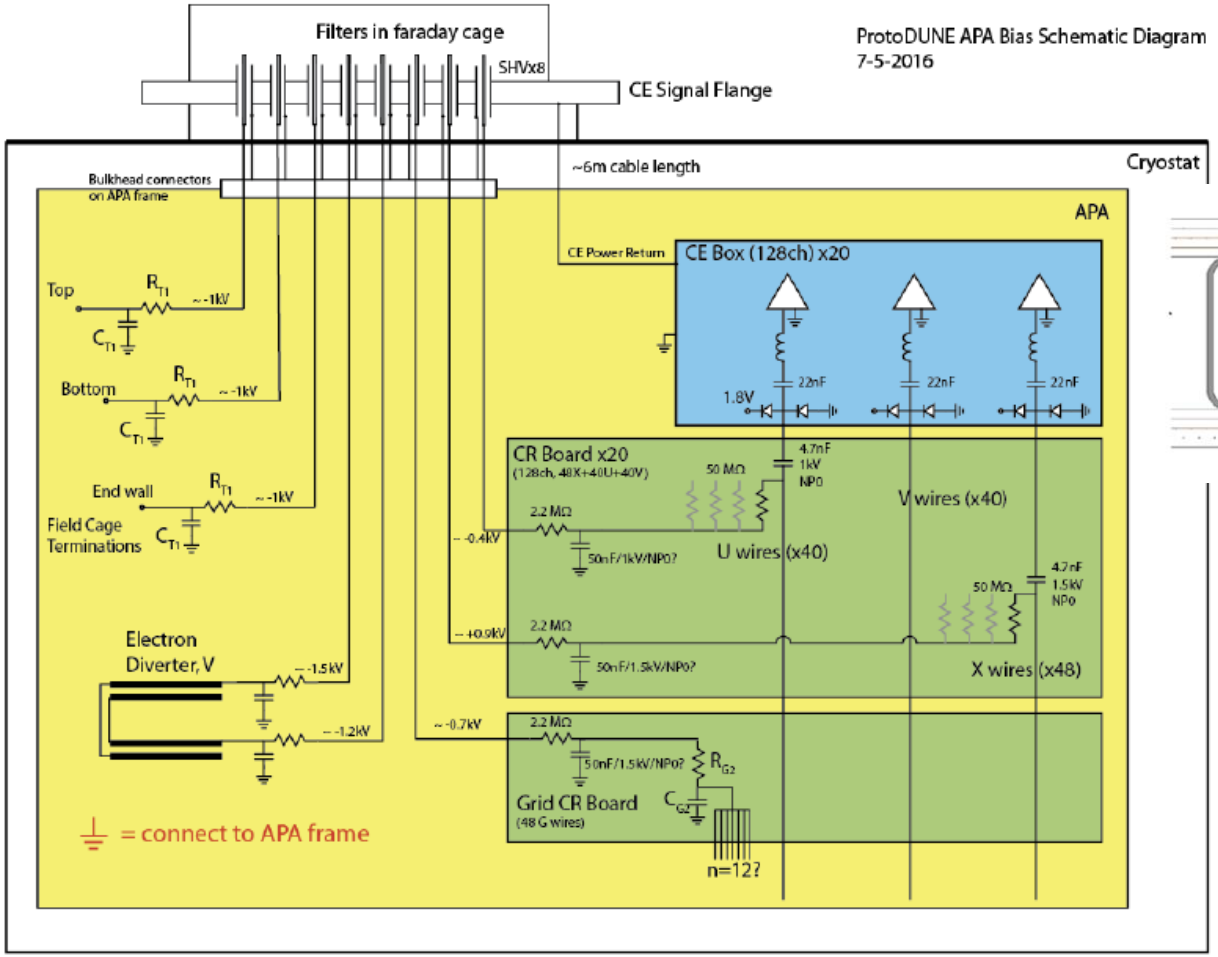


3. COLDATA

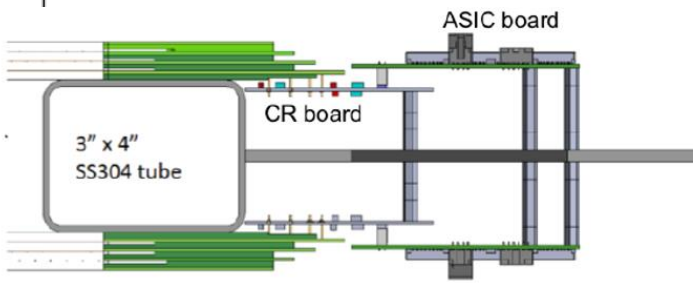
- All communication between the CE on FEMBs and warm electronics, It has 2 x1.28Gb/s line for data transfer and low speed interface for configuration and monitoring plus a line for clock and commands input.

Both COLDATA and Cold ADC are implemented in TSMC 65nm CMOS2 using **cold transistor models** produced by Logix Consulting

Connections from Wire to Front-End



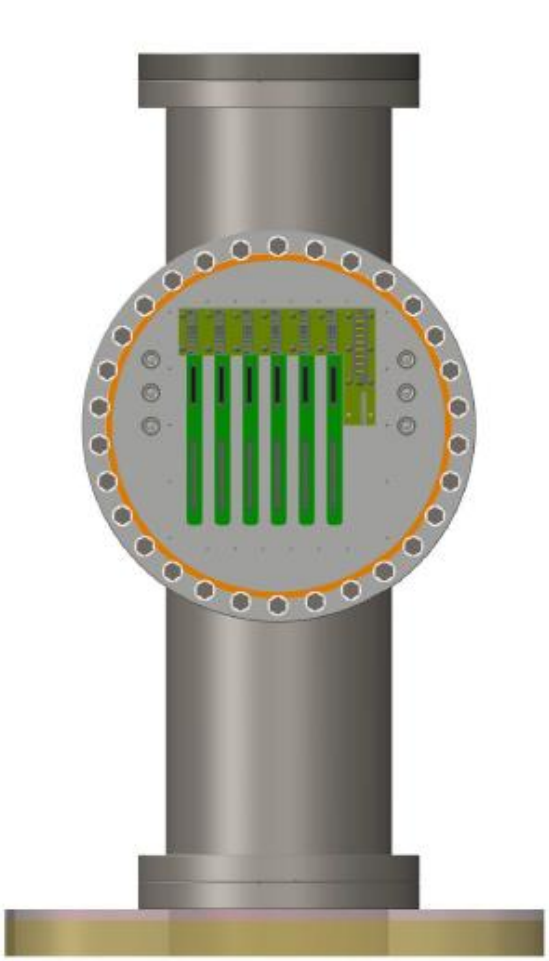
ProtoDUNE-SP APA wire bias schematic diagram, including the CR board.

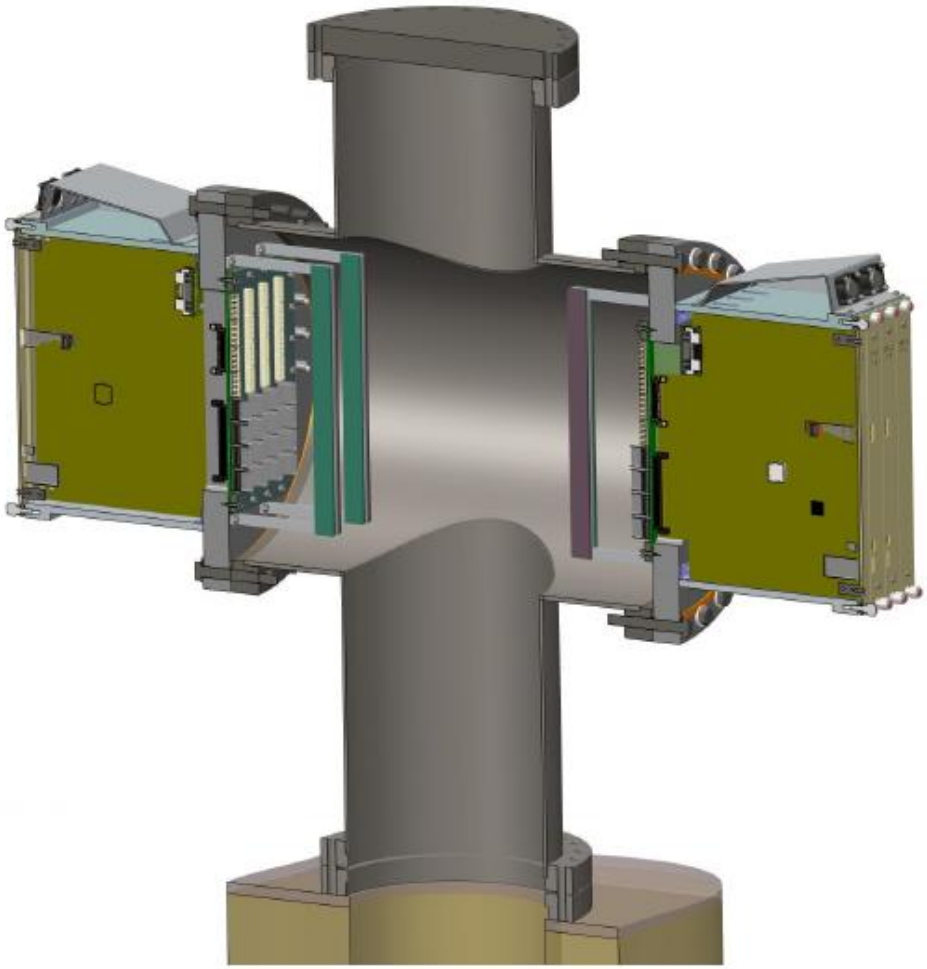


The capacitive-resistive (CR) boards carry a bias resistor and a DC-blocking capacitor for each wire in the X and U-planes.

SP Cold Electronics Feedthroughs and Cold Cables

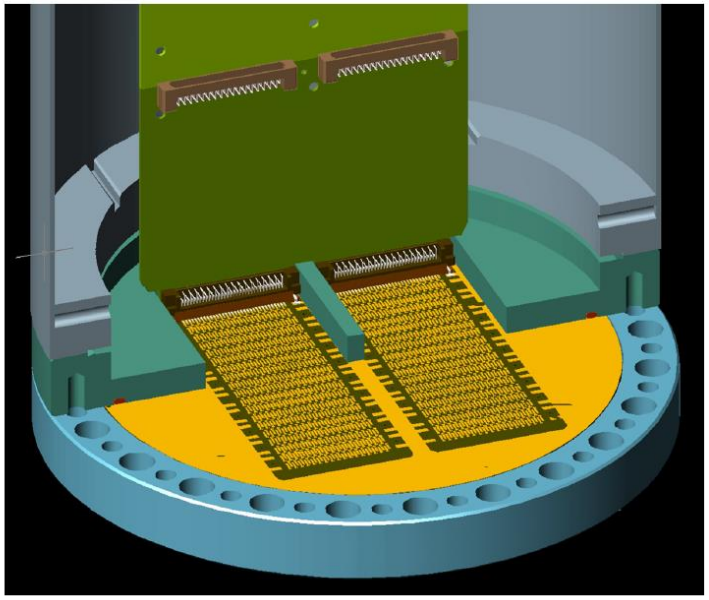
- TPC CE feedthrough. The WIBs are seen edge-on in the left panel, and in an oblique side-view in the right panel, which also shows the warm crate for a SP module in a cutaway view.



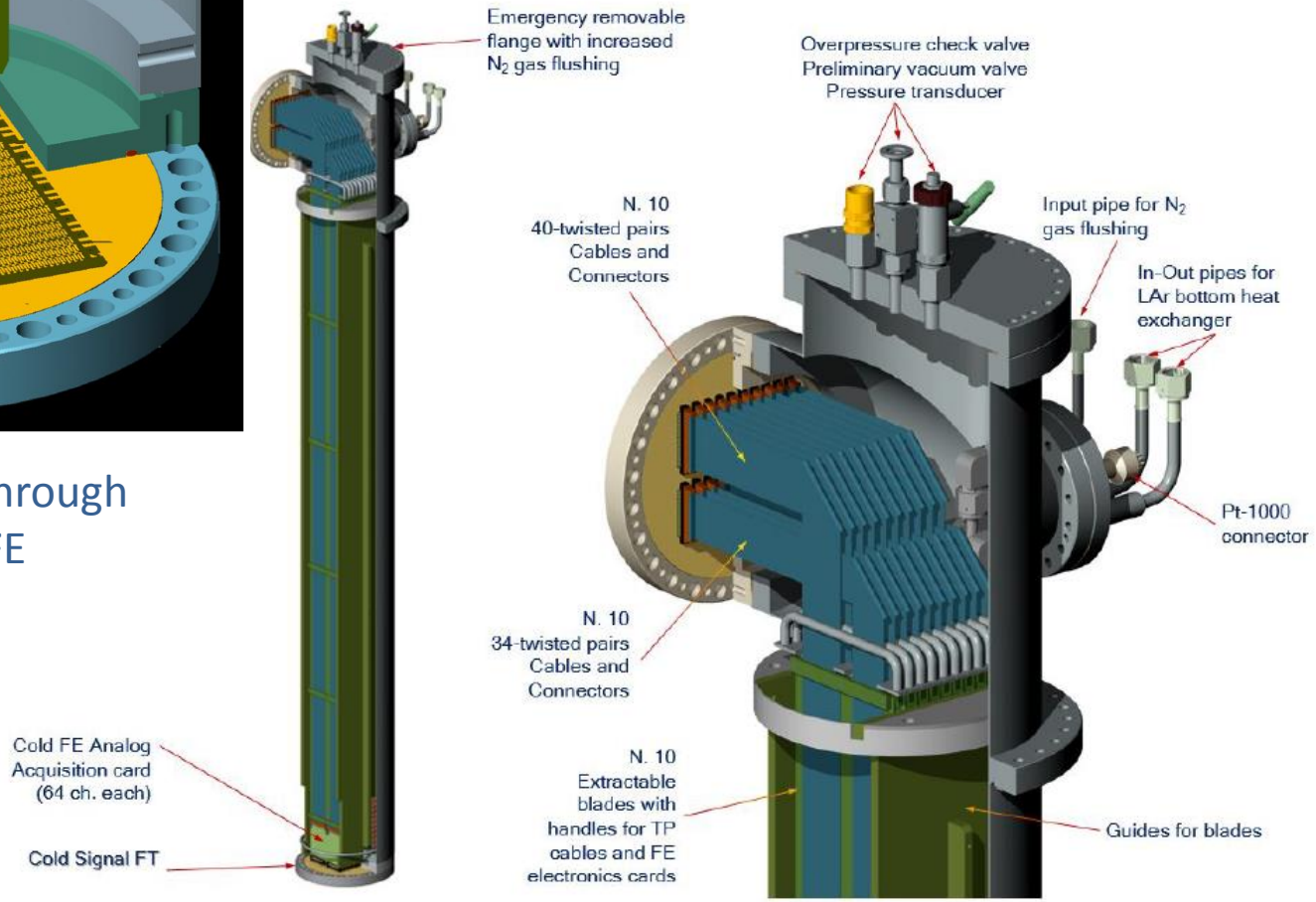


DP Chimney Feedthroughs (SFT)

- Details of the signal feedthrough (SFT) chimney design.

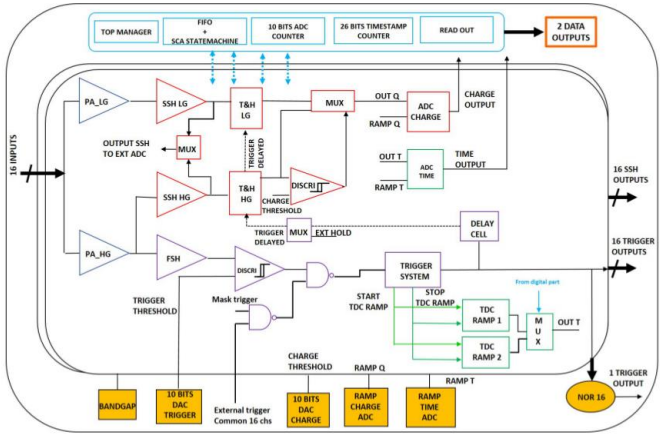


SFT chimney cold feedthrough flange with one of the FE cards mounted



DP - TPC Light Readout 2

- **Waveform branch**
  - The main characteristics of the ADC used for continuous digitization of the PMT signals are shown in table.
- **CATIROC branch**
  - The CATIROC is a 16 channel ASIC dedicated to measurement of charge and precision timing of negative-polarity PMT signals. It auto-triggers on single photoelectrons and can sustain a high dark rate of up to 20 kHz/channel.
  - Charge measurements are possible over the range of 160 fC - 70 pC (corresponding to approximately to a range of 1 to 400 photoelectrons with a PMT gain of1 × 106). Timing measurements per channel can reflect an accuracy of 200 ps.



Item	
Channels	16
Sampling	65 MSPS
Resolution	0.122 mV
Dynamic range	14 bit/ 2 V
Differential non-linearity	typical ±0.6 LSB with min. −0.9 and max. 1.6 LSB
Integral non-linearity	typical ±0.9 LSB with min. −3 and max. 3 LSB

DP module

- The DP module with cathode, PMTs, FC and anode plane with SFT chimneys.