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Electronics for E61 multi-PMTs

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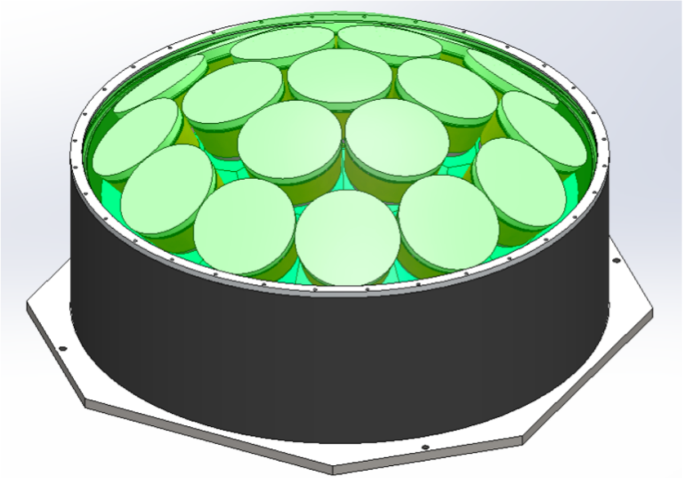
- E61 mPMT
- mPMT electronics requirements
- FADC digitization design



- Other digitization options being explored
- Plan to also use same/similar mPMTs for Hyper-Kamiokande, but this talk will focus on E61.

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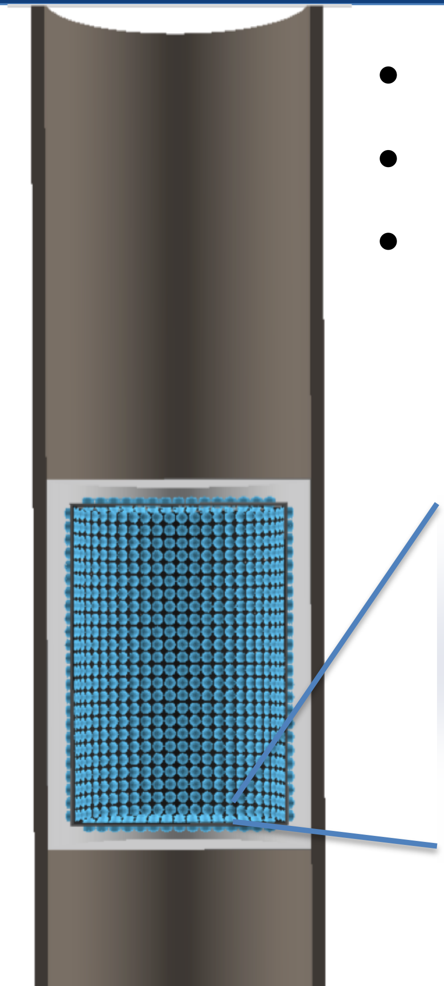
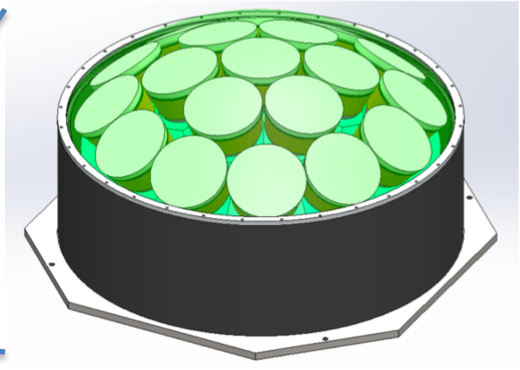
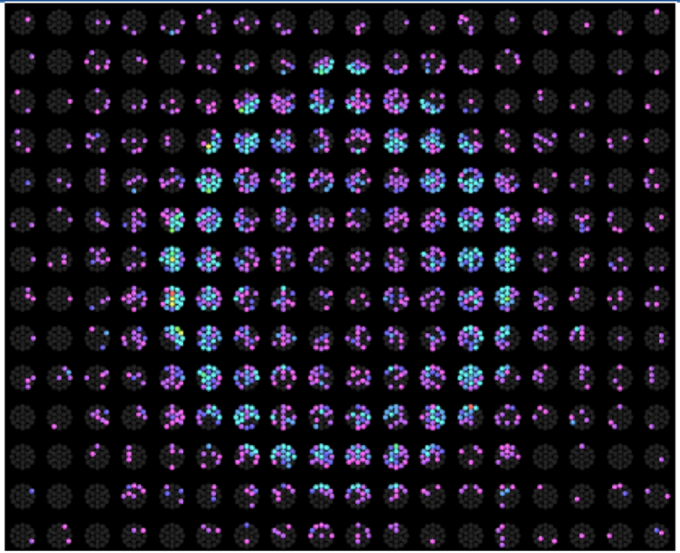
E61 Concept & E61 mPMT



- E61: WC detector.
- Hyper-K near detector
- Measure neutrino interactions at different off-axis angles

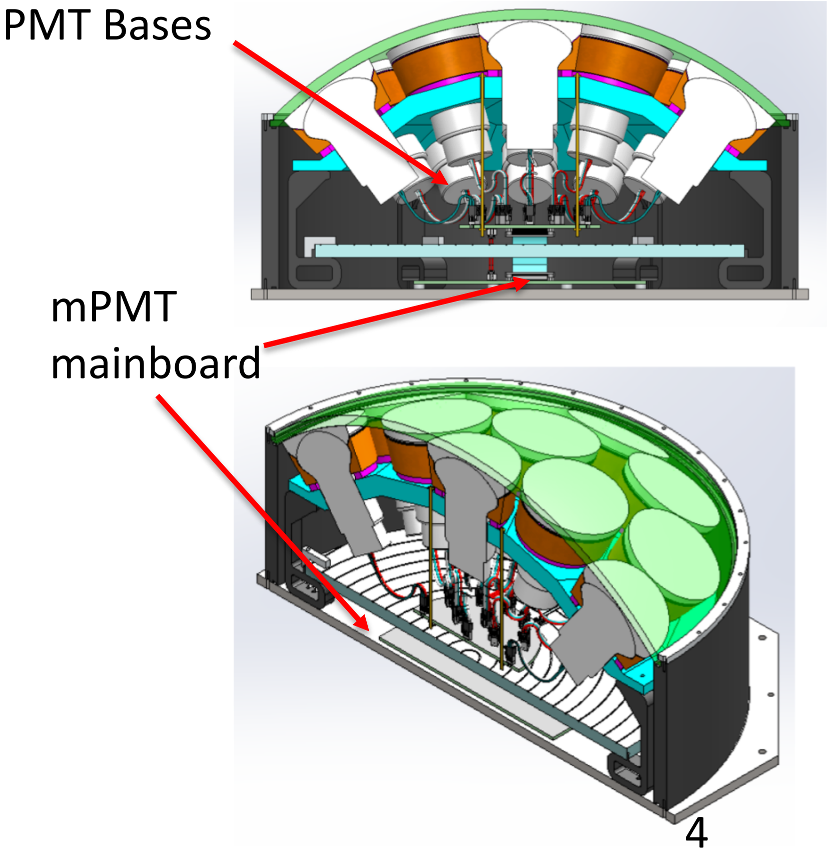


E61 multi-PMT (mPMT) concept (adapted from KM3NET design)



- Use mPMTs for E61 photosensors
- ~500-1000 mPMTs
- Better granularity for small WC detector (4m radius).

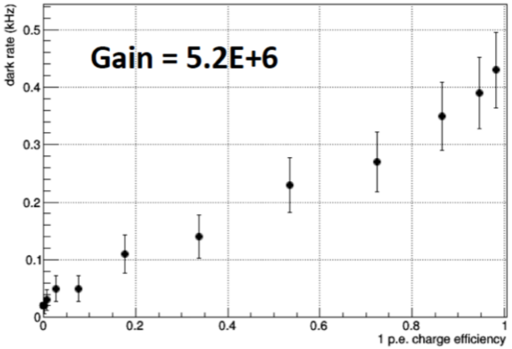
- Need electronics for 19 3" PMTs facing towards inner detector.
- In-water electronics: too many cables/penetrations to route every PMT signal to surface.
- Re-use KM3NET scheme for PMT HV (generate on PMT base).
- Develop new digitization: KM3NET single time-over-threshold does not give sufficient information for large pulses.



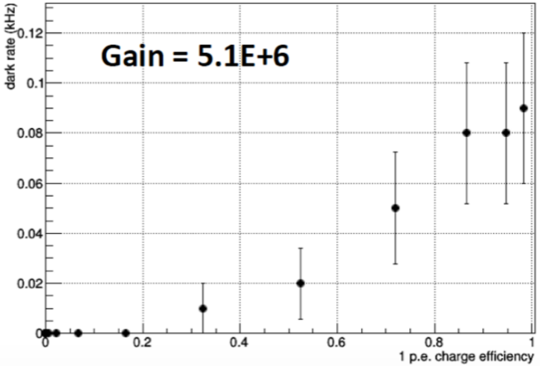
- KM3NET HV generation done on PMT base with Cockroft-Walton circuit.
  - Low power
  - Negative HV on PMT
- But negative HV has higher dark noise rate. Bad for some Hyper-K physics.
- Investigating designs for active PMT bases with positive HV. Some technical challenges to solve.
- Also looking at shielding and coatings to reduce the dark noise rate for -HV.

Dark noise tests at York (Toronto)

R14374, S/N BC0032, -HV



R14374, S/N BC0036, +HV

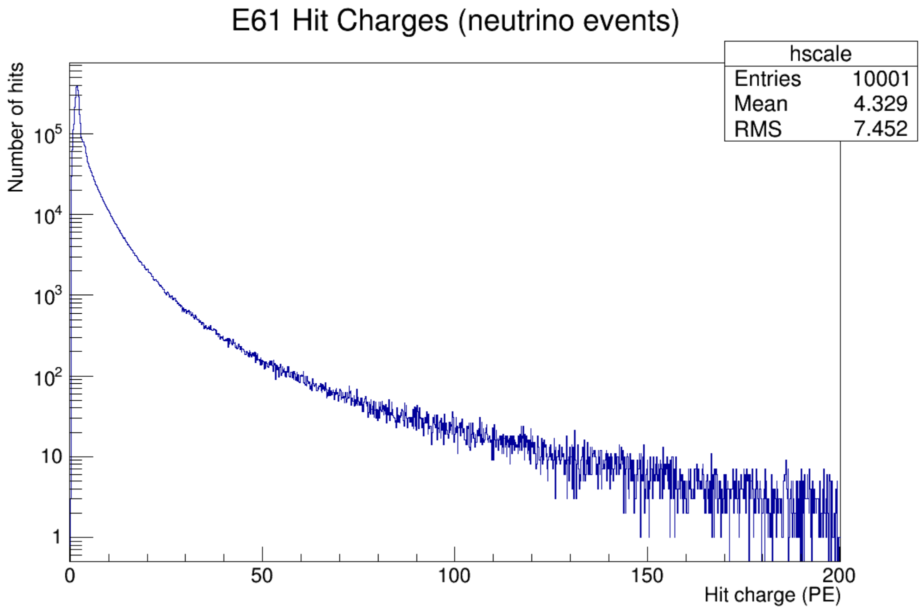


- Performance Requirements
  - Timing resolution: better than 3” PMT TTS
    - 3” PMT TTS (σ) ~0.6ns for 1 photo-electron (PE).
    - So require ~300-500ps timing resolution from electronics for 1PE.
    - Also require better timing resolution (100-200ps) for large PE pulses.
    - E61 Vertex resolution strongly depends on hit timing resolution.
  - Charge resolution ~0.05PE up to 25PE.

E61 Dynamic Range Requirements

Dynamic range requirements: single PE up to 50-100PE

- Simulations show:
  - 0.49% of hits > 50PE
  - 0.13% of hits > 100PE
- Need study of how much saturated hits would effect energy reconstruction.

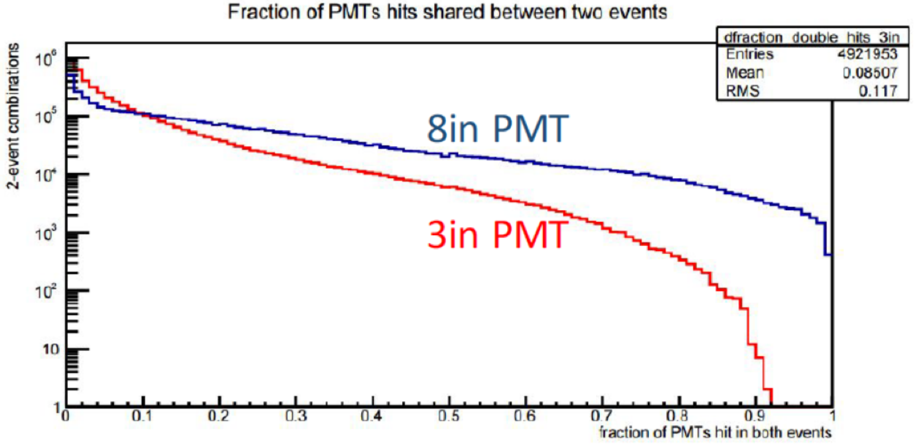


Simulated number of PE per hit for E61 neutrino interactions (improved higher-eff 3" PMTs)

E61 Pile-up/Dead-time Requirements

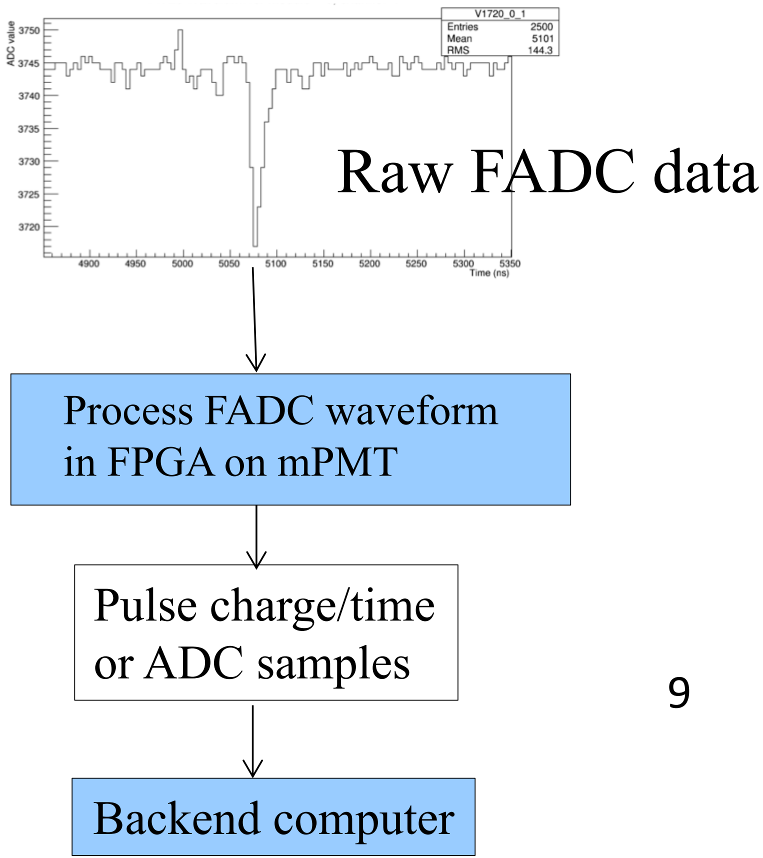
- J-PARC beam spill structure:
  - 8 bunches of ~15ns width, separated by ~600ns.
  - Spill every 1-2 sec.
- Up to 10% of bunches will have two fully contained events (after outer detector veto) for 1^0 off-axis position.
- Single PMTs will often get hit multiple times in the same spill and sometimes multiple times in the same bunch.
- Ongoing studies on separating different events in same bunch.
- At a minimum we need separate measurements for each bunch. Finer time information would be better.

\# of pmts hit twice in both events/
# of pmts hit

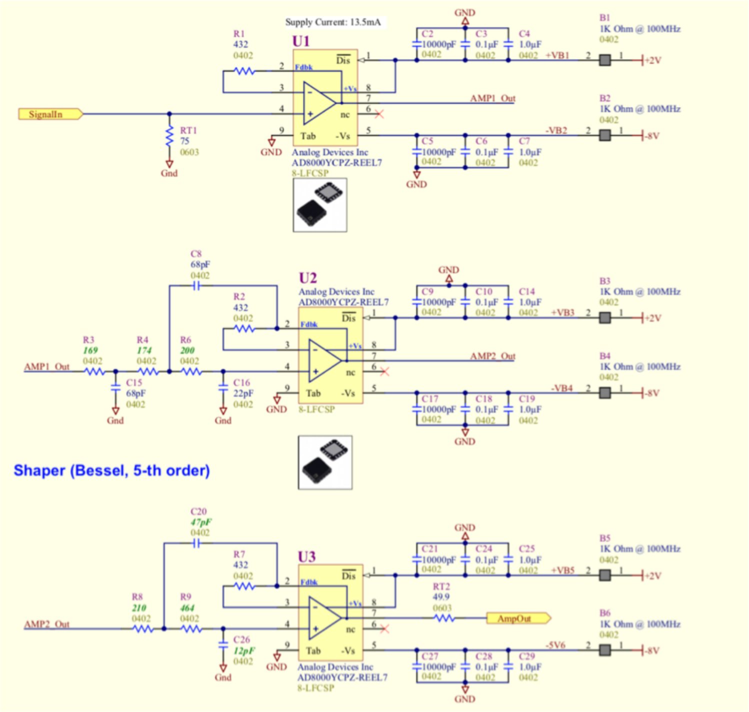


FADC Digitization Overview

- FADC continuously processed with FPGA; finds hits and send pulse summary to backend.
  - Pulse summary is either just Q/T and quality factor (for small pulses) or a set of ADC samples (for large pulses).
- FPGA data processing also allows for more sophisticated techniques for noise suppression.
- Challenges:
  - Ensure we can meet timing resolution and dynamic range requirements.
  - Possibly high cost & power.

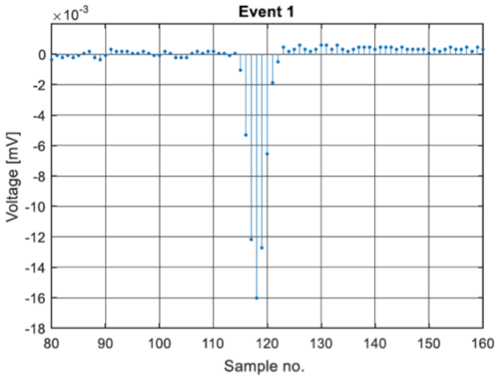


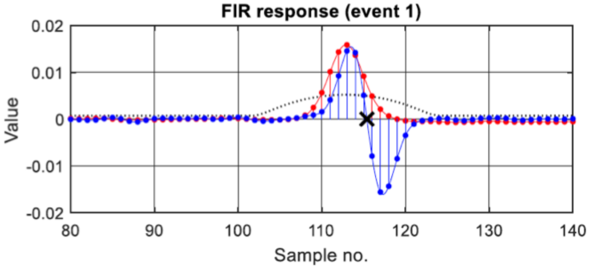
- Current shaper design:
  - 5-th order Bessel filters (smooth impulse response)
  - Optimized for 100 MSPS system, with rise time of 15 ns or 30 ns.
- Still optimizing design and considering other options.



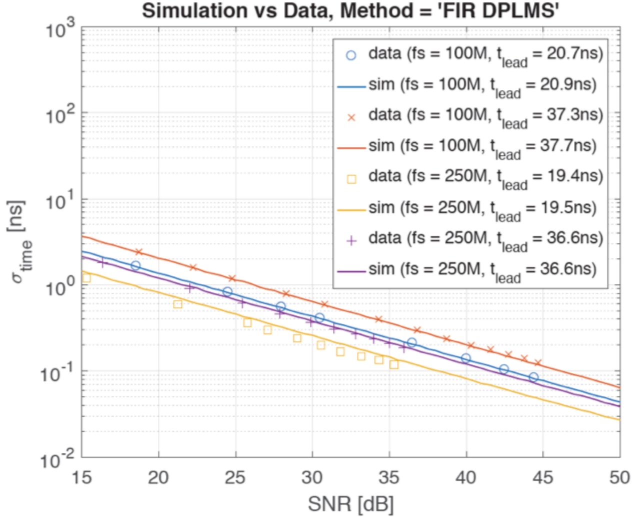
Techniques for extracting hit time

- Tested different techniques for extracting hit time.
- Constant Fraction Discriminator or Finite Impulse Response (FIR) can be implemented in FPGA (fits cannot).
- Find that FIR filtering gives timing resolution that is slightly worse than by fitting pulses.
- Also find that our data is well described by simulation.



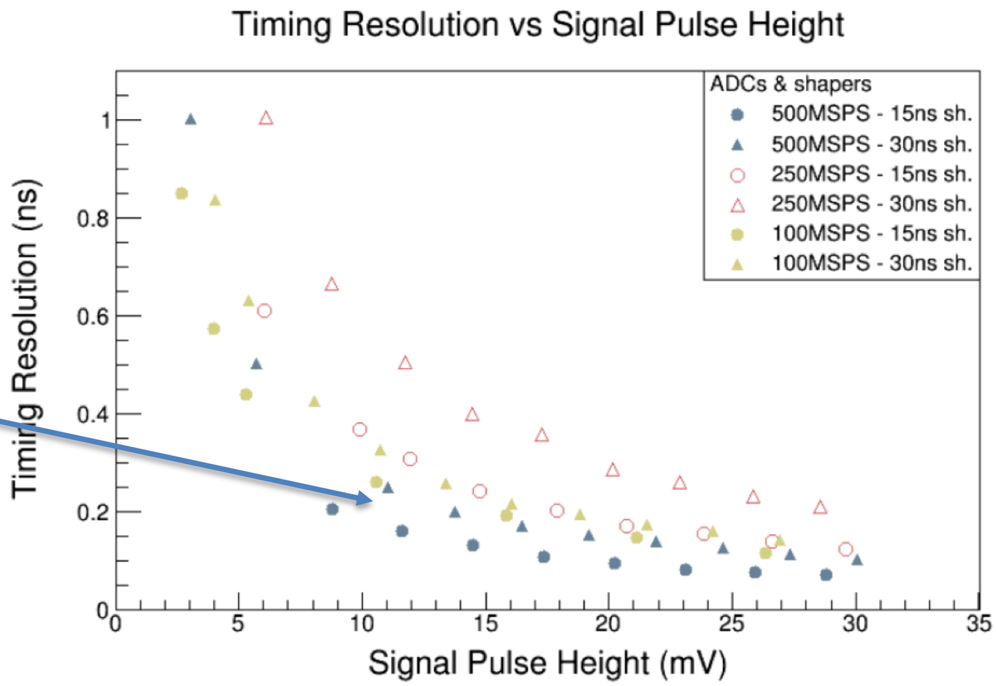


Timing resolution using FIR filtering on waveform



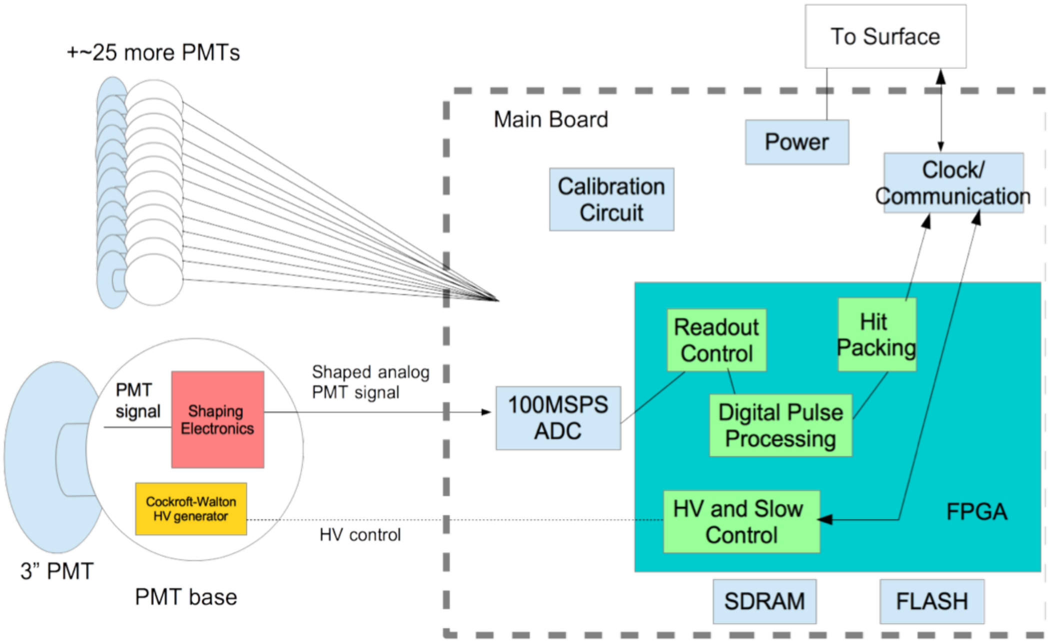
Timing Resolution for FADC Digitization

- Tests of performance with different CAEN ADCs:
  - 100MSPS 14bit
  - 250MSPS 12 bit
  - 500MSPS 14 bit
- Assume 1PE pulse is 10mV high; achieve <0.5ns timing resolution from electronics.
- With 2V ADC get 0-200PE dynamic range.
- **100MSPS ADC meets timing and dynamic range requirements.**



FADC Electronics Design

- 100—200MSPS ADC on mainboard.
- Need to test that cable doesn't degrade noise performance.
- Plan to produce prototype over next year.
- Power: aim for ~100mW per channel for ADC.
  - ~5W for overall mPMT electronics.

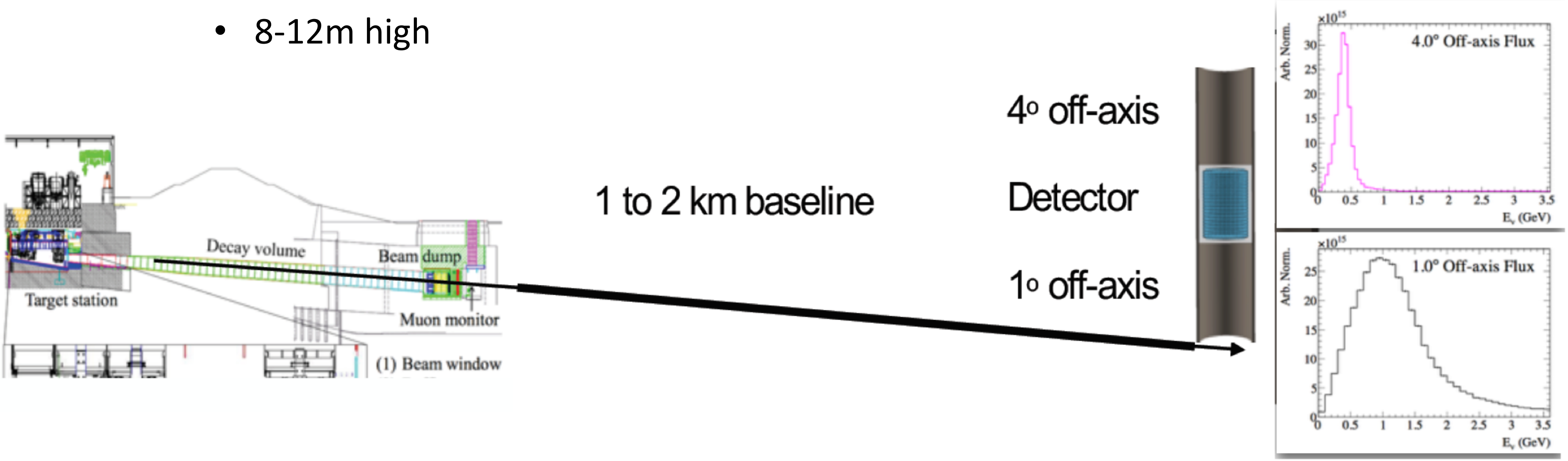


Conclusion

- Key requirements for E61 digitization: achieving deadtime-less readout for 5us beam spill and sub-nanosecond timing resolution.
- Working on digitization design based on 100MSPS FADC digitization.
- Work to be done if we want to use positive HV with an active PMT base.

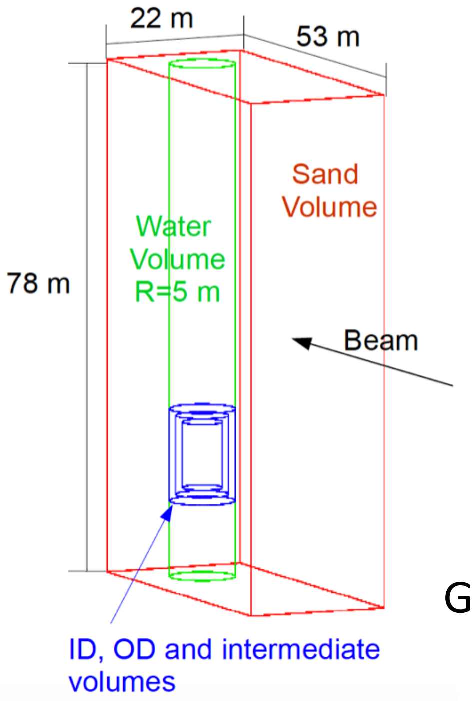
E61 concept

- Measure neutrino interactions at different off-axis angles -> different energy spectrums.
- WC detector moves up/down in 50m shaft.
  - Detector:
    - 8m diameter inner diameter
    - 8-12m high



Event rates per microbunch for E61 with horn currents at 320 kA and ID radius of 4 m before any cuts.
For detector at 1km from production target.

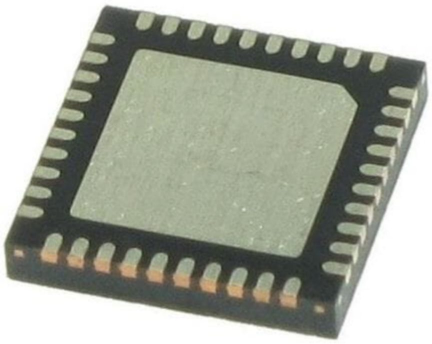
	Interaction Outside OD			Interaction Inside OD			Interaction Inside ID		
	Producing light in:								
Off-axis Angle (°)	OD only	ID only	ID & OD	OD only	ID only	ID & OD	OD only	ID only	ID & OD
0.0-0.6	0.612	0.004	0.488	0.763	0.007	0.265	0.008	0.807	0.479
1.0-1.6	0.193	0.001	0.147	0.227	0.002	0.079	0.002	0.227	0.134
2.0-2.6	0.061	0.000	0.044	0.077	0.001	0.026	0.001	0.084	0.042
3.0-3.6	0.025	0.000	0.016	0.033	0.000	0.011	0.000	0.036	0.015



Geant4 pile-up simulation

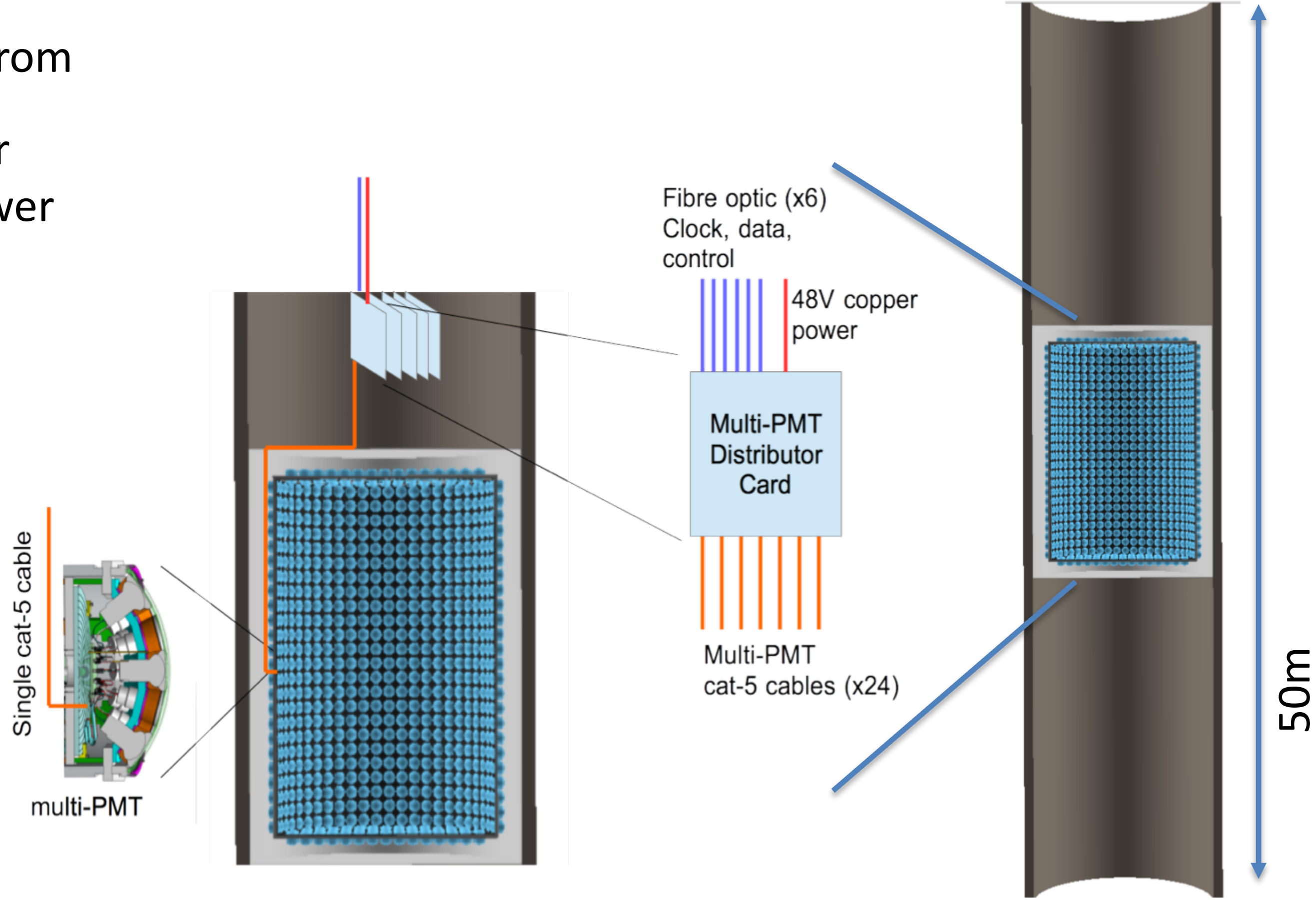
- TI ADC 3424
- Quad 125MSPS ADC
- 12 bit (11.4 ENOB)
- Power 98mW per channel
- ~$17 USD per channel

- AD LTC2260-12
- Single 125MSPS ADC
- 12 bit
- Power 146mW per channel
- ~$36 USD per channel



E61 Cabling Concept

- Single cat-5e cables from mPMT to distributor board above detector
- Combined signal/power cables up to surface

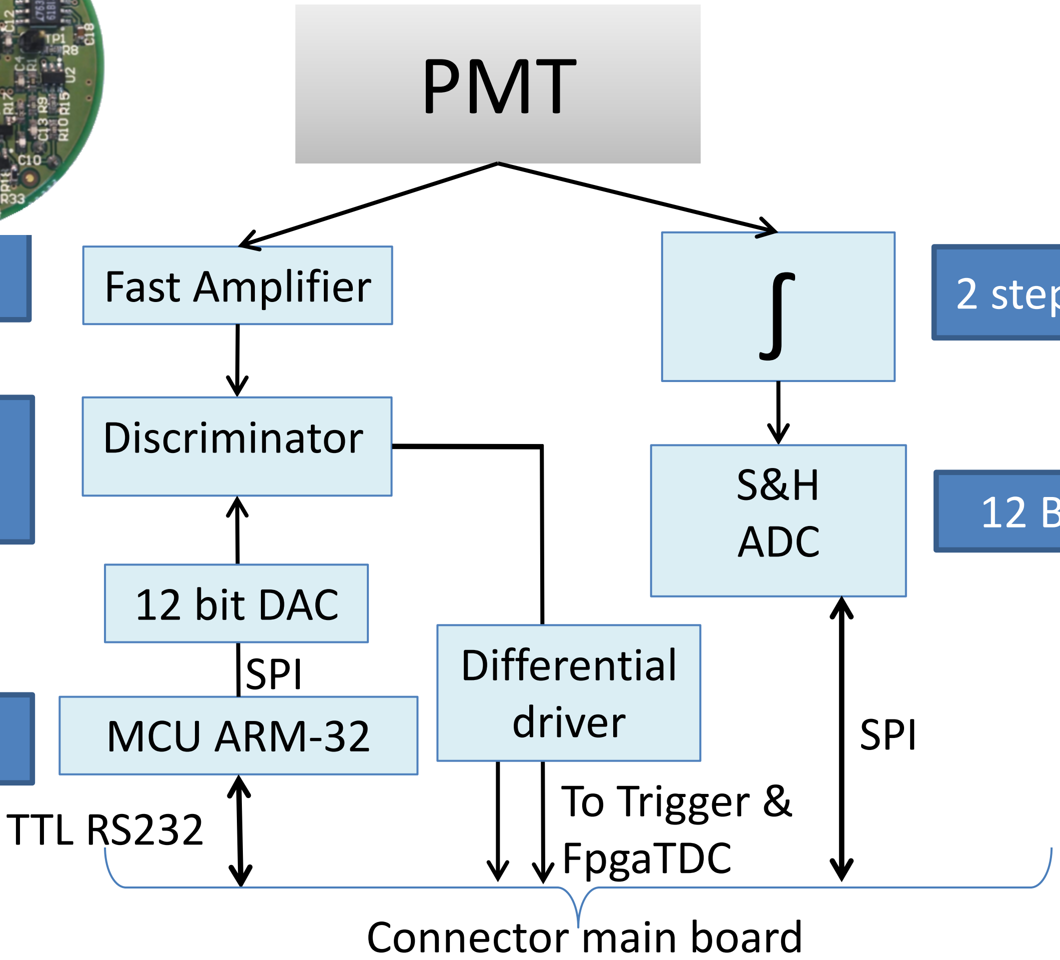


Alternate Digitization Block Diagram

2 step amp: Gain ~ 60

Fast comparator
4.5 ns propagation delay

0-2.5 V Threshold
(0.6 mV step)



2 step integrator

12 Bit 2 MSPS

- Prototypes available for PMT base, FEB and mainboard.