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# DAQ for Fall 2018 Run

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# Overview

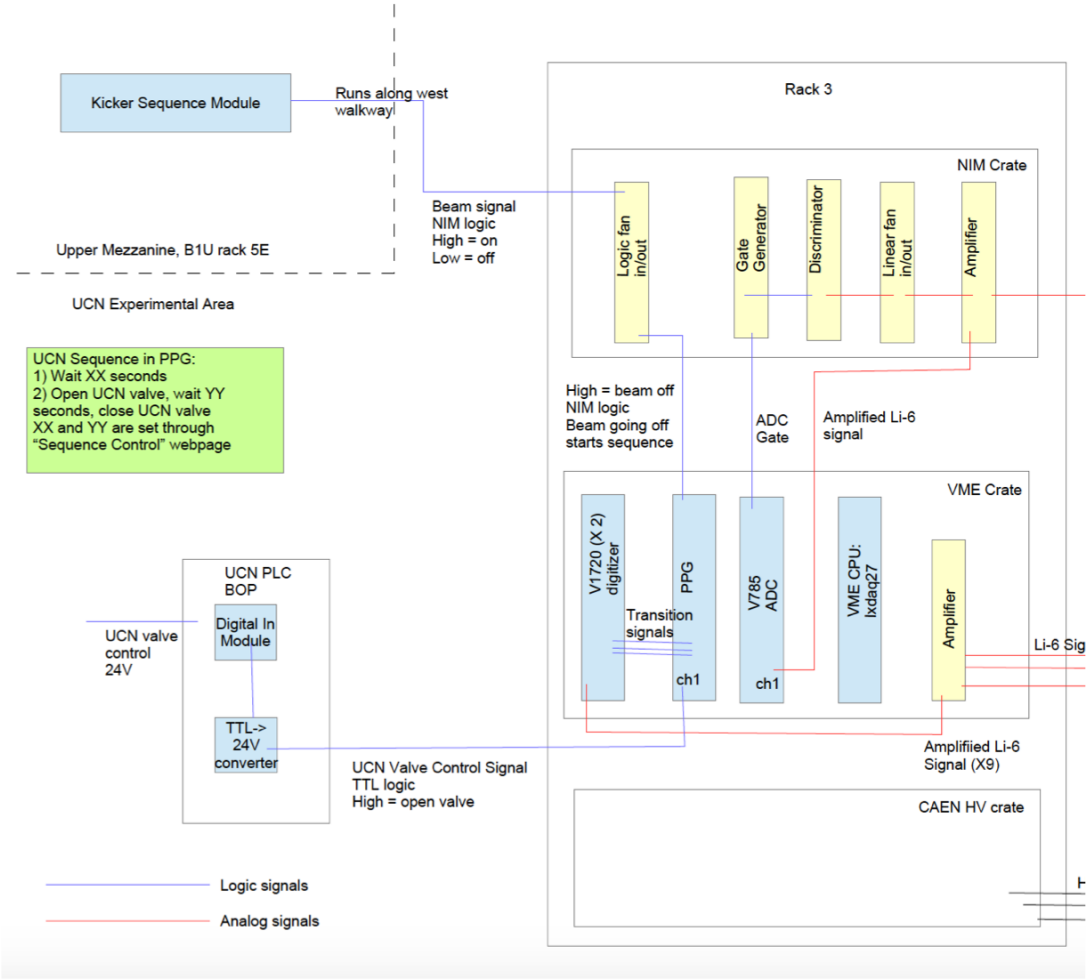
DAQ Task list for 2018 run

- New gate control
- Add timing of gate valves
- Clean up sequencer controls

# Valve Control

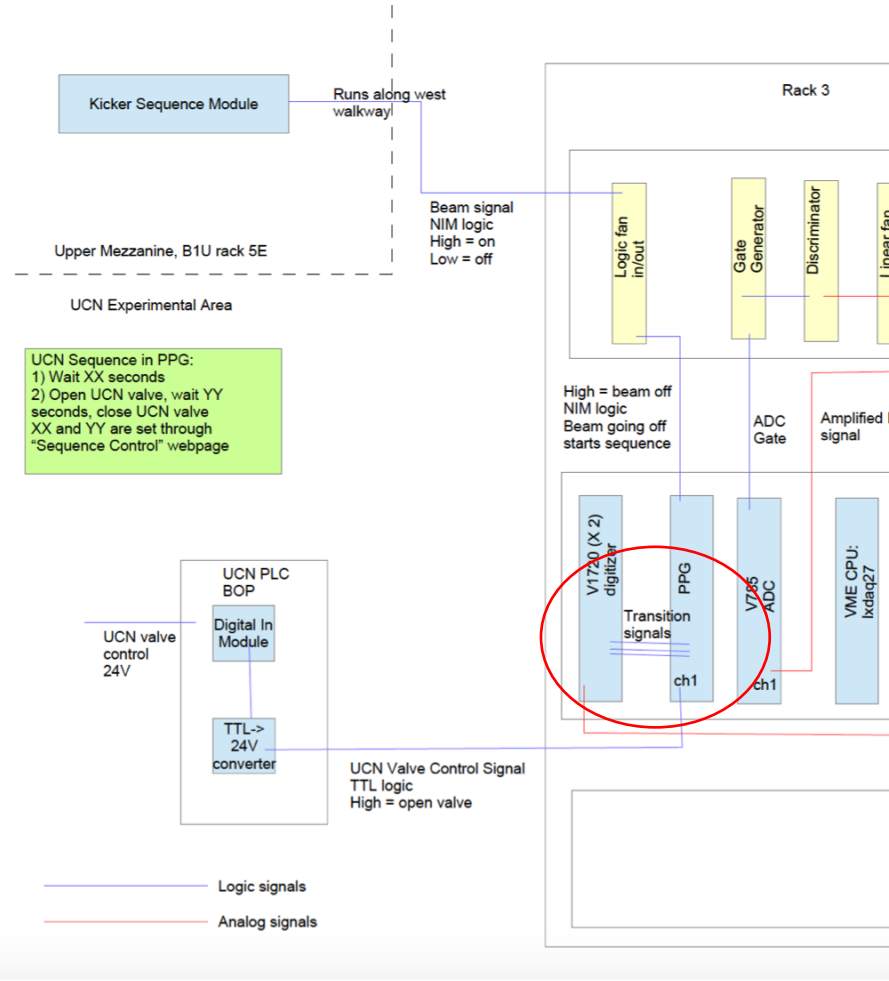
- UCN Valve control (2017)
  - Open and close initiated by VME sequencer card.
  - Control signal converted from TTL to 24V and fed into PLC
  - Control signal copied and sent to Li-6 V1720

- Repeat for N more valves. Need
  - Cables between VME crate and PLC.
  - New PLC code and wiring.
  - Don't have enough extra channels in V1720 digitizer to handle extra valve control signals.



# Improved Timing Measurements

- There aren't enough spare channels in V1720 to record signals from 4 more gate valves.
- Need to add some other card to record when the other valves open/close. Options:
  - MCS
  - Chronobox (used by ALPHA-G)
- Would other card be synchronized to same clock as V1720? Hopefully.
  - Otherwise injecting one gate signal into both V1720 and other card to synch them.
- We also will try to signal back from PLC that indicates exactly when the valves finish opening and closing. Could be useful to monitor that.
  - Need to think about how to implement that.



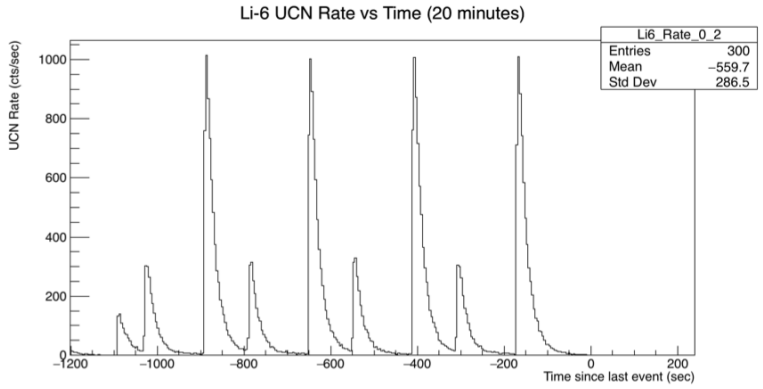
# Improve Controls & Fix Bugs

- Need to update the sequencer control page to add extra valves.
- How complicated, flexible to make the system for setting up valve sequences?
  - Possibly simple sequences get set through webpage and complicated sequences get set through scripts.
- Did we write up list of DAQ problems from last year?  I will need some reminding of the bugs that we wanted to fix.
- Also need better online monitoring, so we catch these problems at the time…

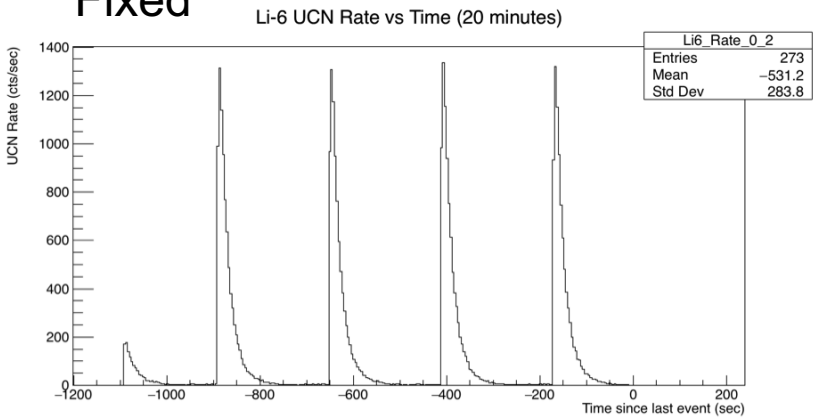
# V1720 Clock roll-overs

- Problem with shifted hits is caused by missing the 17s clock roll-over on V1720 digitizer
- In case Steve noted (run 814) missed 8 clock roll-overs for second V1720 board.
- Possible to fix for 2017 data… but need to figure out how to automate the fix.
- For 2018 run, should investigate again whether we can get the new V1720 firmware working that has longer timestamps.

Raw

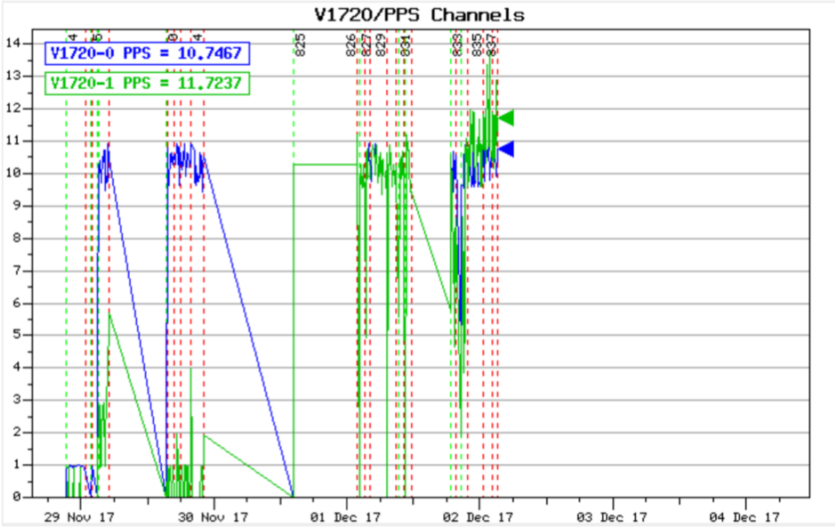



Fixed



# V1720 Clock roll-overs

- Tried to avoid this problem by injecting a pulse-per-second signal into last channel of each V1720.
- But somehow this didn't work for second V1720 for this period.
  - possibly related to recalibrating V1720 baselines.
  - Somehow got fixed after Dec 1st, but can't find record of what was done.
- This problem is visible in history plots… need to add this to the hourly checks.
- Still not totally clear why the problem didn't affect all the runs in this period (Nov 29-31)



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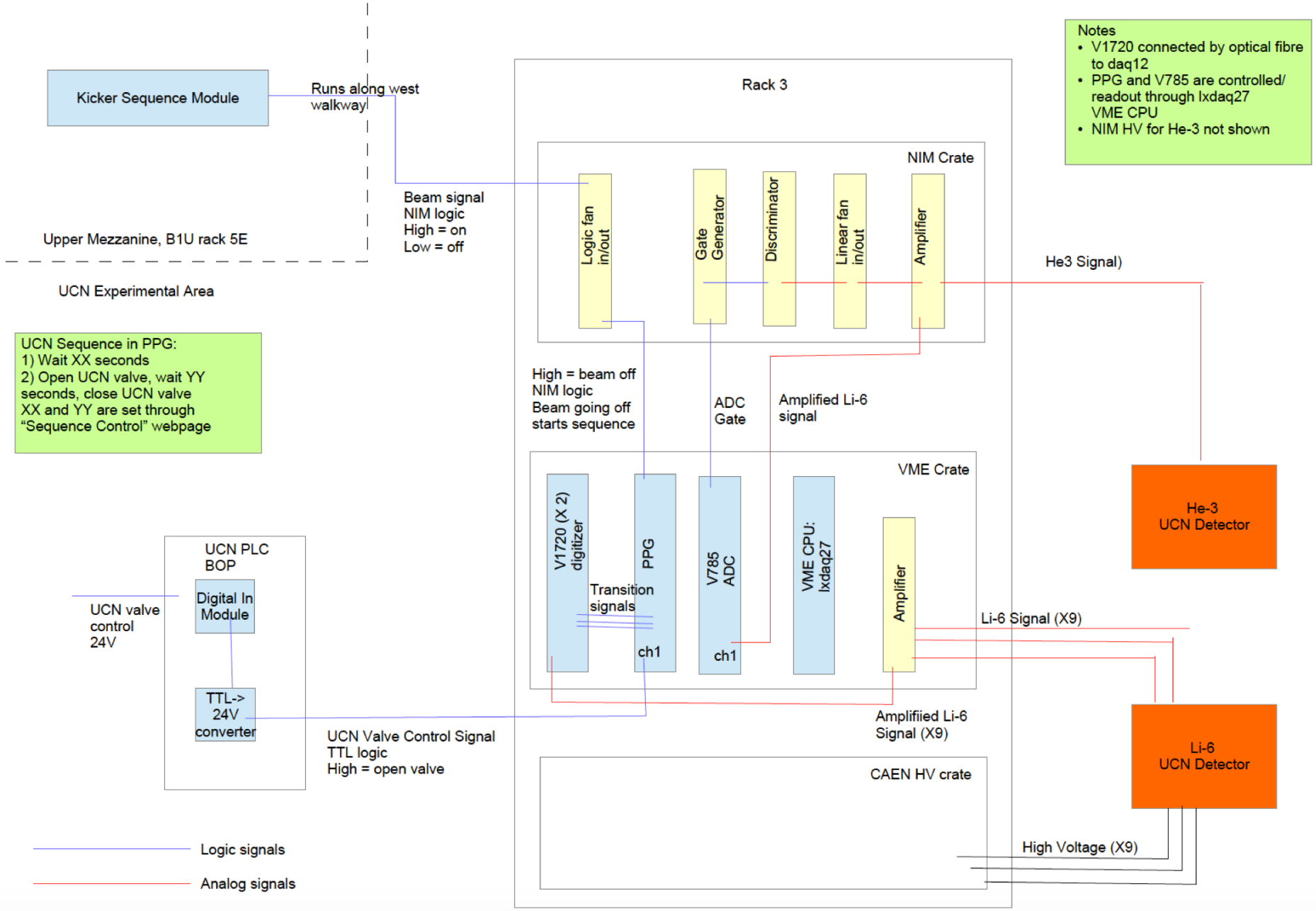
# Backups


Notes
• V1720 connected by optical fibre to daq12
• PPG and V785 are controlled/ readout through lxdaq27 VME CPU
• NIM HV for He-3 not shown
Kicker Sequence Module
Runs along west walkway
Upper Mezzanine, B1U rack 5E
UCN Experimental Area
Beam signal NIM logic High = on Low = off
Rack 3
NIM Crate
Logic fan in/out
Gate Generator
Discriminator
Linear fan in/out
Amplifier
He3 Signal)
UCN Sequence in PPG:
1) Wait XX seconds
2) Open UCN valve, wait YY seconds, close UCN valve
XX and YY are set through "Sequence Control" webpage
High = beam off NIM logic Beam going off starts sequence
ADC Gate
Amplified Li-6 signal
VME Crate
V1720 (X 2) digitizer
Transition signals
PPG
ch1
V785 ADC
ch1
VME CPU: lxdaq27
Amplifier
He-3 UCN Detector
Li-6 Signal (X9)
UCN PLC BOP
Digital In Module
UCN valve control 24V
TTL-> 24V converter
UCN Valve Control Signal TTL logic High = open valve
Amplifiied Li-6 Signal (X9)
Li-6 UCN Detector
CAEN HV crate
High Voltage (X9)
Logic signals
Analog signals