

# Performance of ATLAS Hadronic End-Cap Calorimeter Electronics Chain Configurations

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## HEC Readout Chain

- For the high luminosity upgrade of the Large Hadron Collider (LHC), new application specific integrated circuits (ASICs) have been developed to meet higher signal and trigger rates. This readout electronics upgrade is for the liquid argon calorimeter system.
- The HEC preshaper and shaper ASIC processes signals from the hadronic end-cap calorimeter.
- The HPS ASIC has four channels consisting of a preshaper and two CR-RC2 shapers with low gain (LG) and high gain (HG).
- Tests have been performed on chain configurations involving a preamplifier, the current ATLAS preshaper/shaper, the HPS ASIC, and a full chain configuration using a long signal cable.
- Functional and quality control tests for step response and linearity are used to validate HPS function.

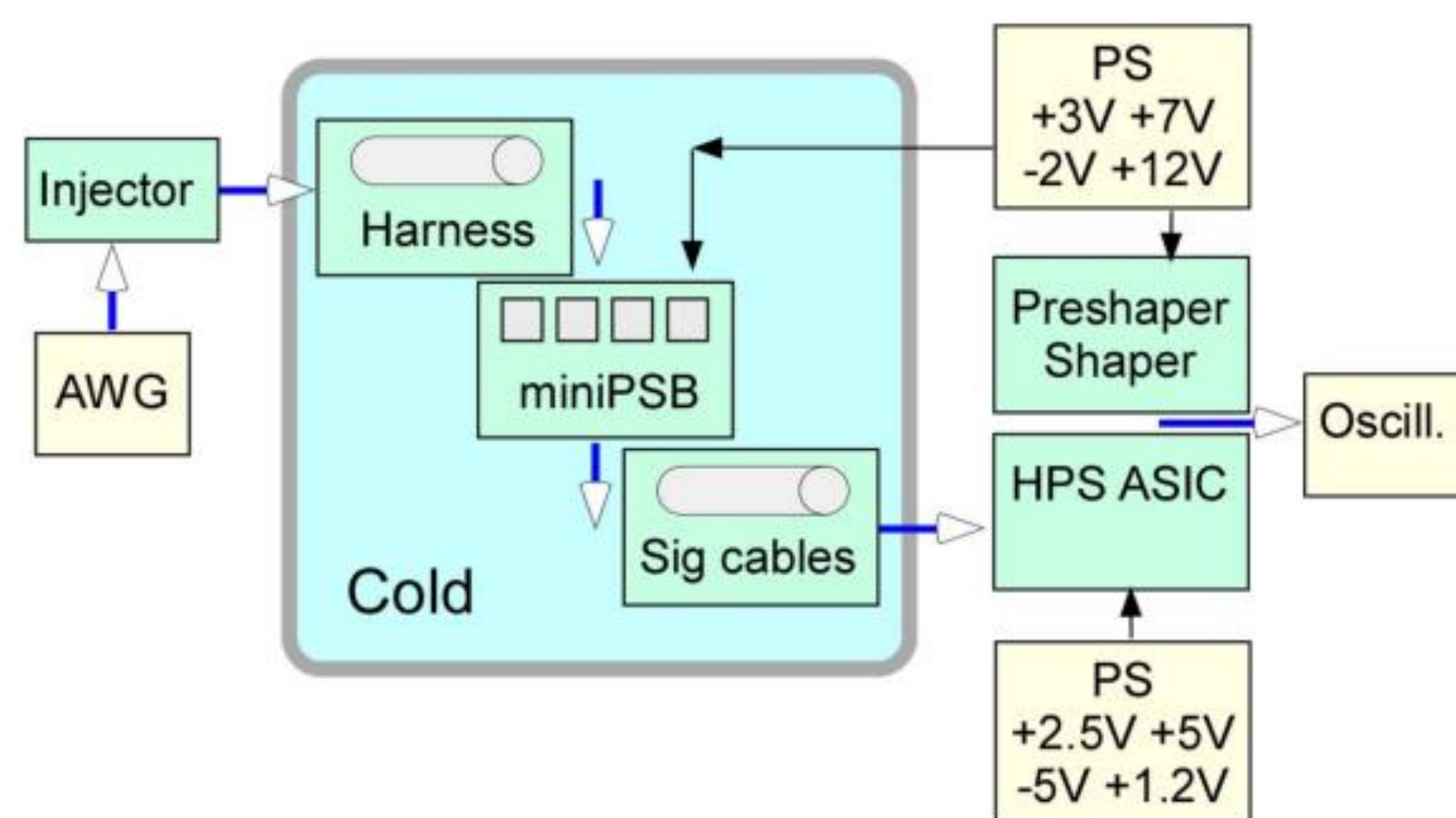


Figure 1. HEC mockup diagram showing configurations used for performance tests and measurements.<sup>1</sup>

## Preamplifier Transfer Function Model

- Step response tests are used to validate the response of the preamplifier to input signals. The simplified transfer function model  $H(t)$  is a convolution function that can be represented in time and frequency domains. The time domain function is given as:

$$H(t) = \frac{G}{\tau_a - \tau_d} \left( e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_d}} \right)$$

- Detector capacitor values determine the signal rise time and noise value. The model includes a gain parameter  $G$  and two poles,  $\tau_a$  and  $\tau_d$ .

In this model,  $\tau_a = (C_d + C_a) \cdot R_{in}$

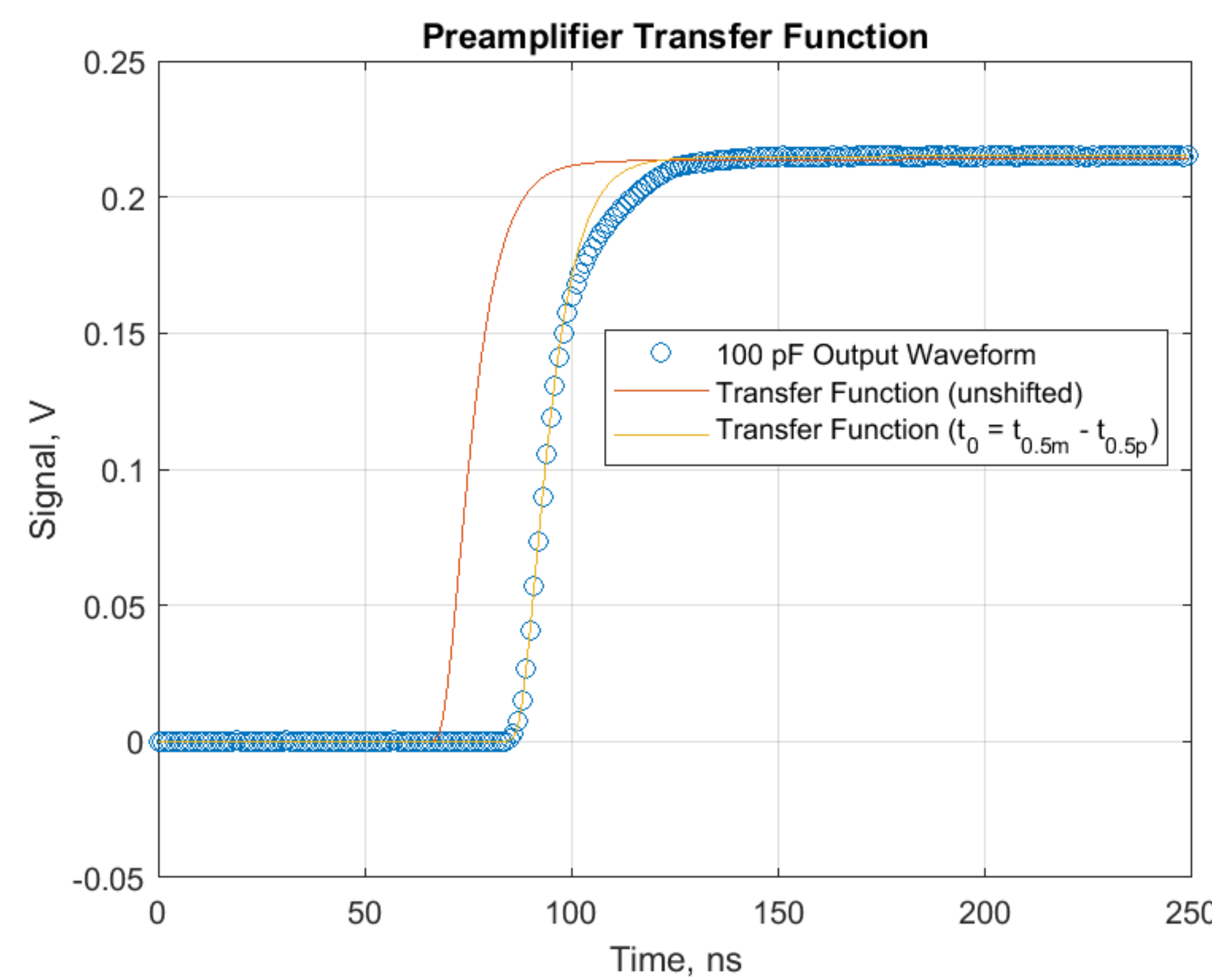


Figure 2. Transfer function model for the preamplifier. Time constant parameter optimization is used for the poles after time delay is accounted for.

- $\tau_a$  increases linearly with increasing detector capacitor ( $C_d$ ) values.  $C_a$  is 50 pF from the first transistor and increases the signal rise time. Input impedance  $R_{in}$  is 50  $\Omega$ .
- Decoupling capacitors are not accounted for in this model, but are present in the ATLAS setup. This introduces a differentiation of the signal, and they make the final signal shape prediction  $\sim 1\%$  more accurate.

## HPS ASIC Shaper Tuning

- The ASIC is programmable with I2C bytes that can be loaded into the HPS. Tests involve two HPS outputs (LG and HG), two preshaper gains ( $G1$  and  $G2$ ), and four  $C_d$  values (100 pF, 150 pF, 220 pF, 330 pF).
- The optimal configuration provides a peak time of  $\sim 50$  ns and a rise time of  $\sim 45$  ns, which is the time between 5% of amplitude to the peak.
- Shaper is first scanned over 8 symmetric time constant settings, then one time constant is varied for fine tuning. The long signal cable in the full chain configuration results in shorter shaper time constants.
- Linearity of the signal amplitude was also measured until a threshold voltage is reached and the shaper output begins saturating. This depends on the preshaper gain and HPS output.

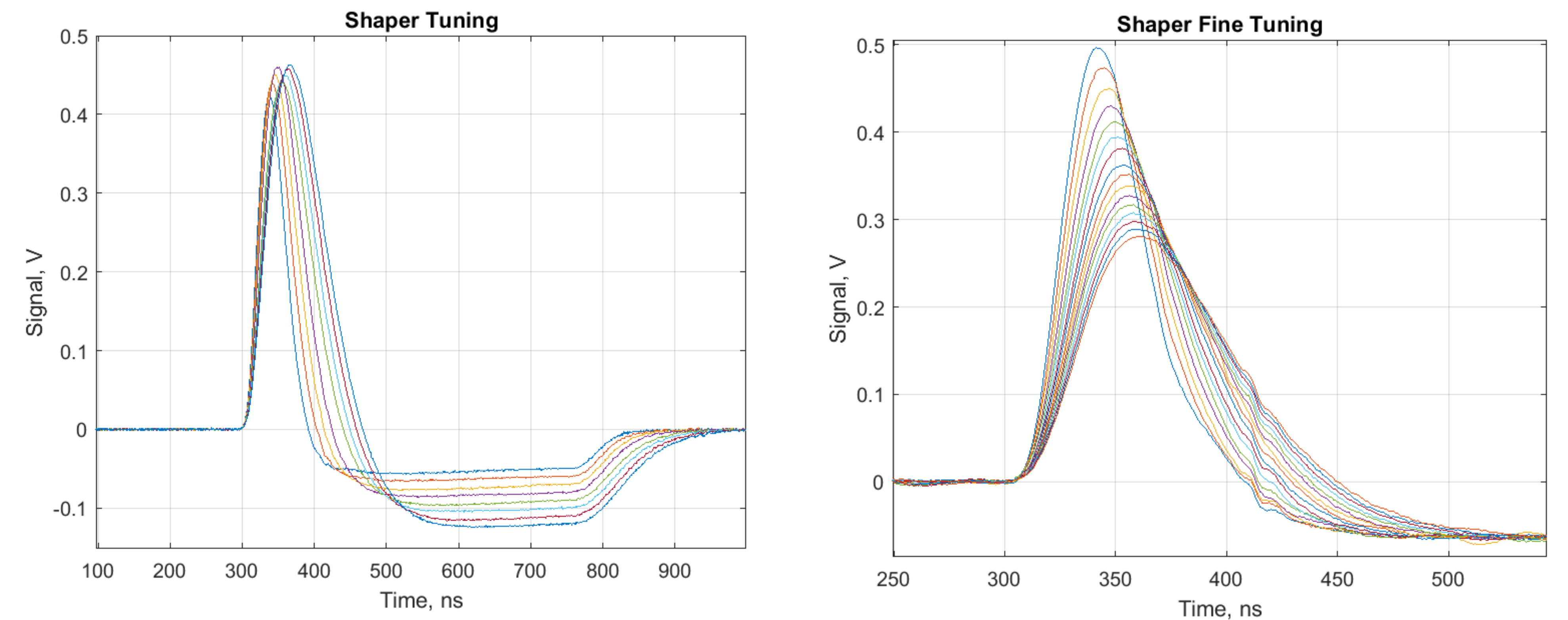


Figure 3. Left: Waveforms from scanning symmetric time constant settings for a 100 pF G2 LG configuration with the HPS ASIC. Right: One time constant is varied, and the rise time is optimized for the same configuration.

## LHC Luminosity and Pileup

- Signals using different luminosities were used to measure noise and pileup. Signals modelled 20 to 200 interactions per bunch crossing, and noise was found to increase. This varied minimally with different  $C_d$  values.

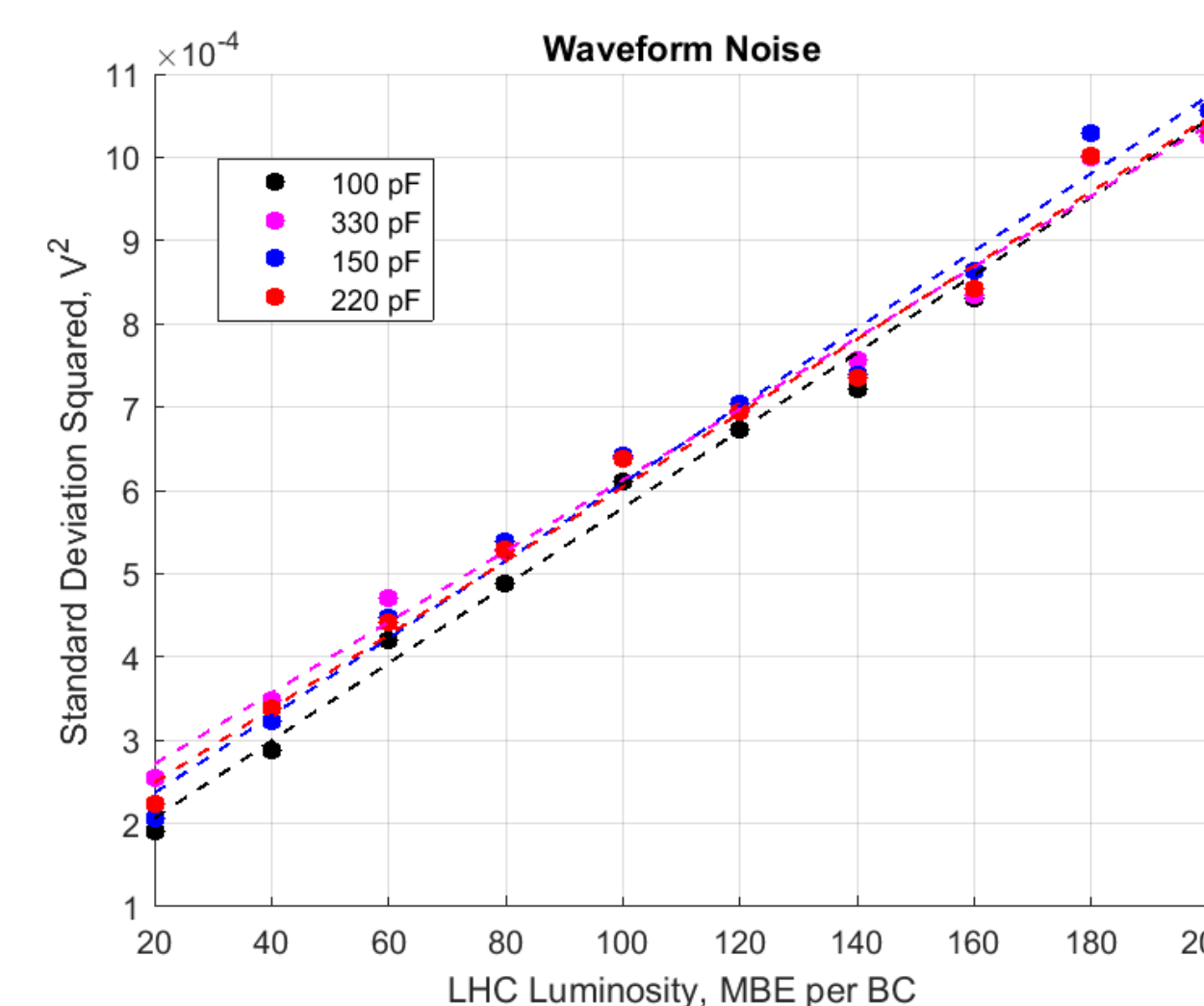


Figure 4. Noise increases with increasing minimum-bias events per bunch crossing. This was tested for four detector capacitor values.

## Summary

- Performance tests were used to investigate the operation of the HPS ASIC that will be used in the high luminosity upgrade of the LHC.
- Validating tests were performed for step response measurements and linearity. The fine tuning of time constants enabled an optimal configuration of I2C bytes to be identified.
- Increasing luminosity was found to increase noise in recorded signals.
- Future work involves quality check and quality assurance tests of HPS pre-production chips with the goal of conducting all characterization tests.