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# PHOTON-TO-DIGITAL CONVERTER FOR LARGE SCALE NOBLE LIQUID DETECTORS AND NEUTRON IMAGING

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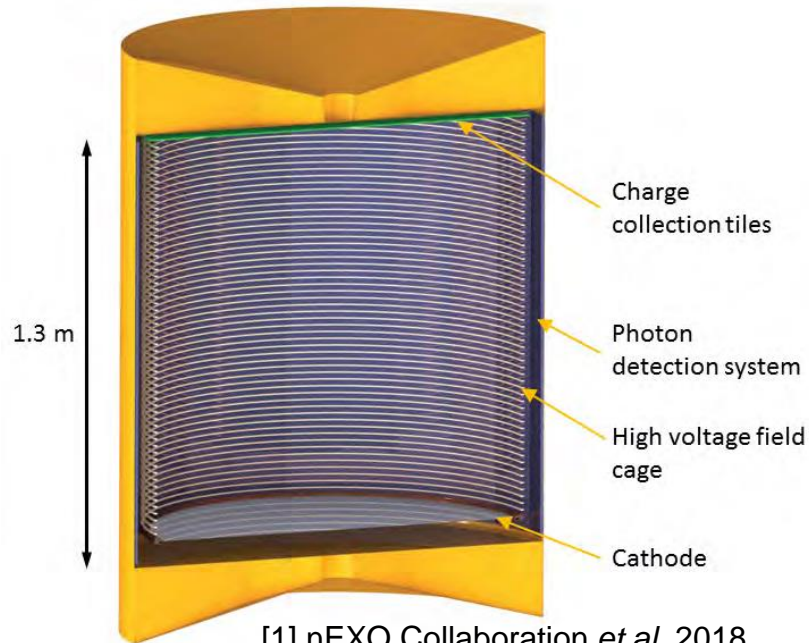
February 15<sup>th</sup> to 18<sup>th</sup> 2024

61<sup>st</sup> Winter Nuclear & Particle Physics Conference



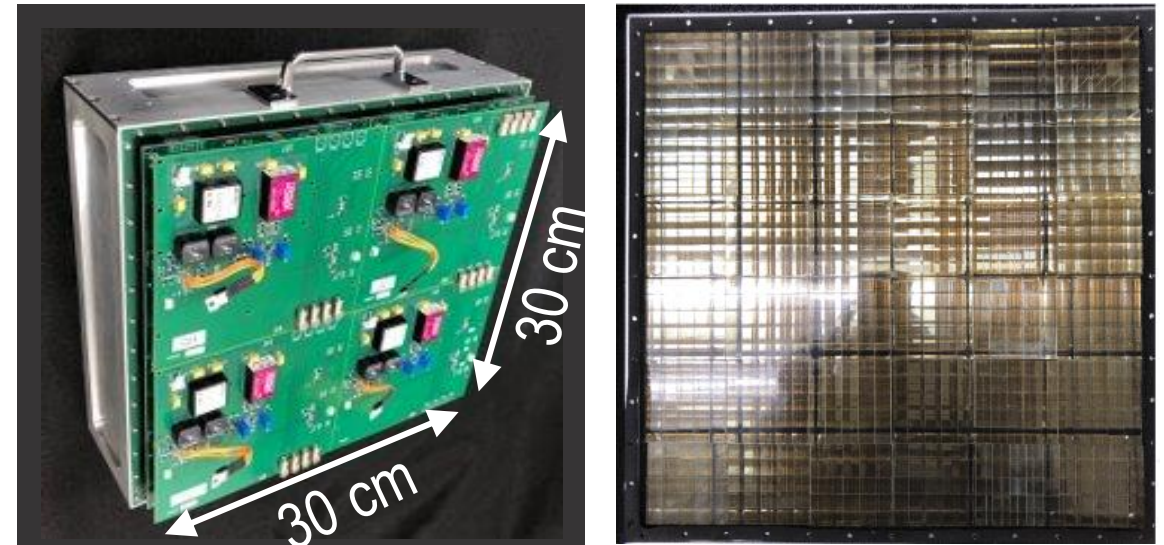
## Large Scale Noble Liquid Experiments

- Neutrinoless double beta decay and dark matter search
- 4.6 m<sup>2</sup> of detectors
- 200 W max.



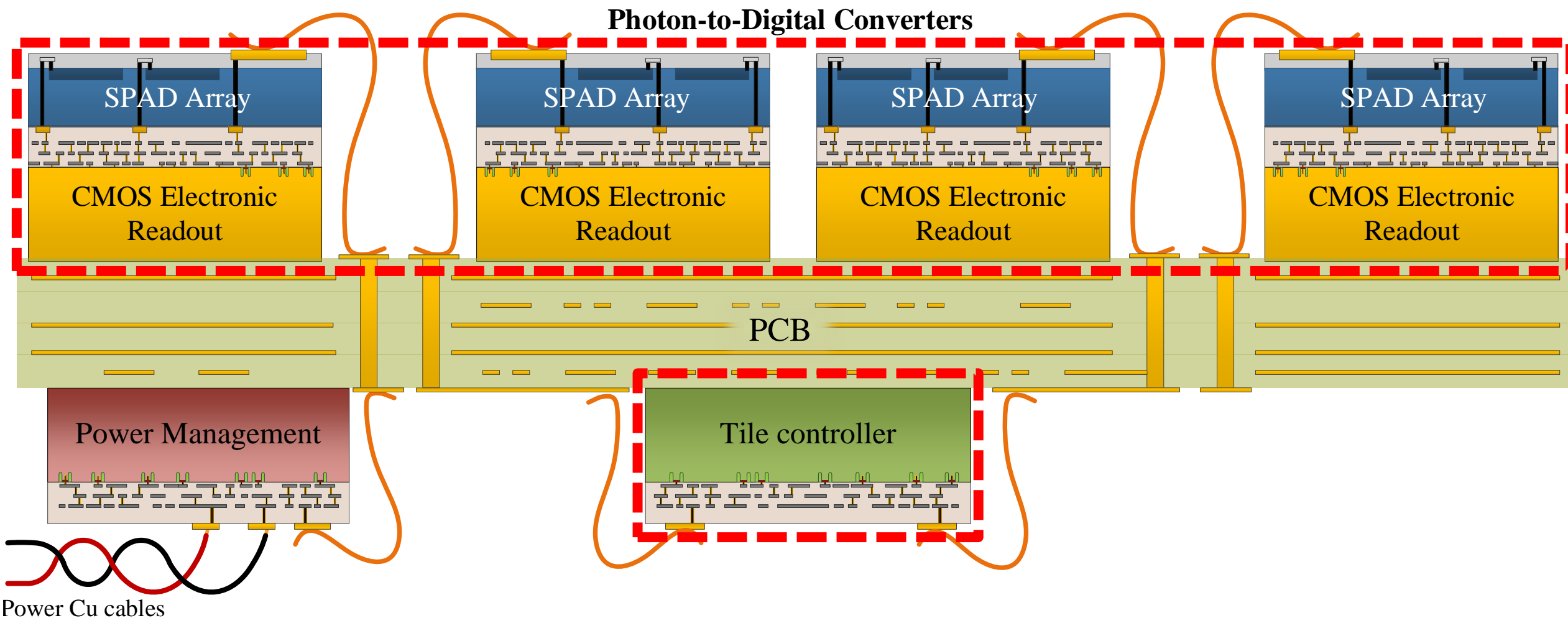
## Neutron imaging

- Large pixelated sensitive area
- Portability (compact and low-power)

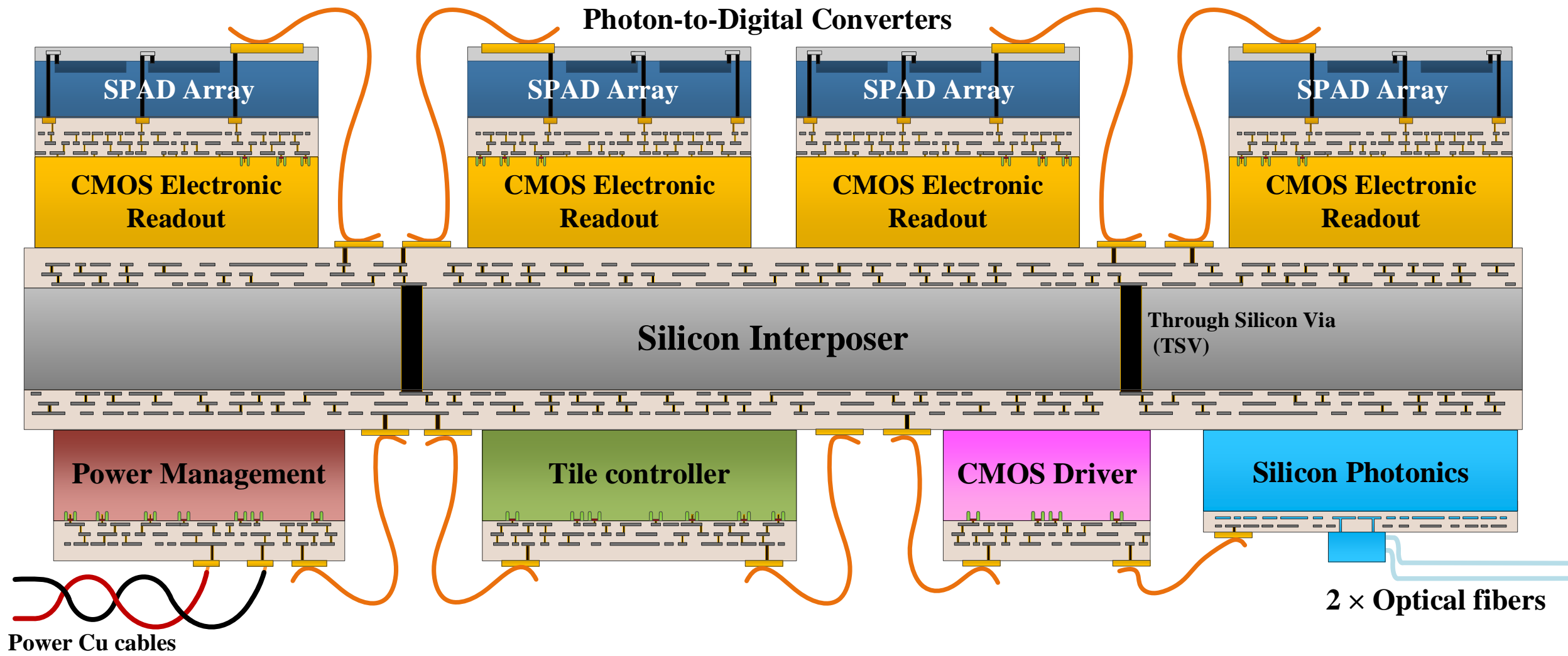


ORNL Portable Pixelated Fast-Neutron Imaging Panel [2]

**Need : Large area, low-power and good timing precision photon counting system.**

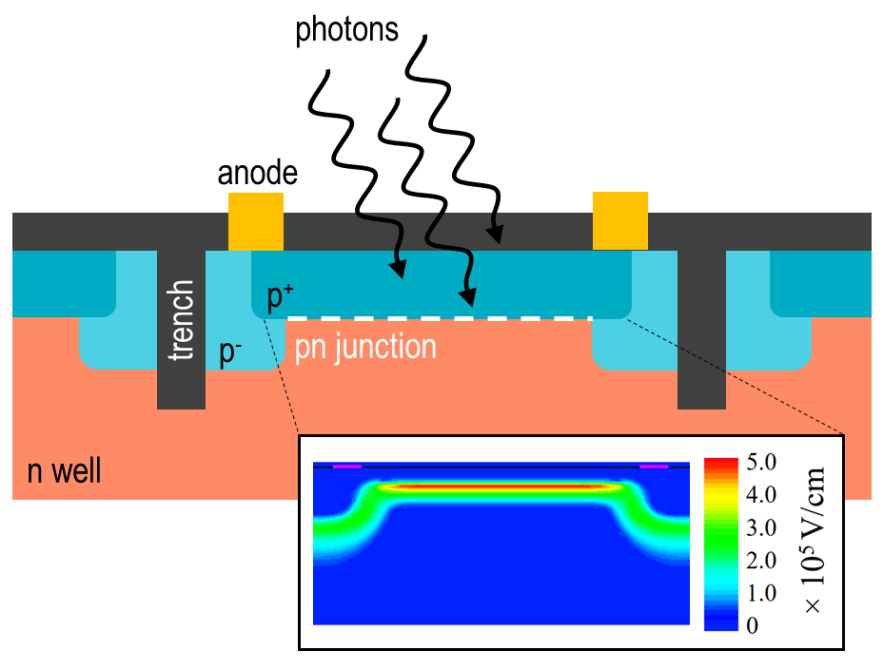


# DIGITAL SOLUTION: 3DPDC + TILE CONTROLLER

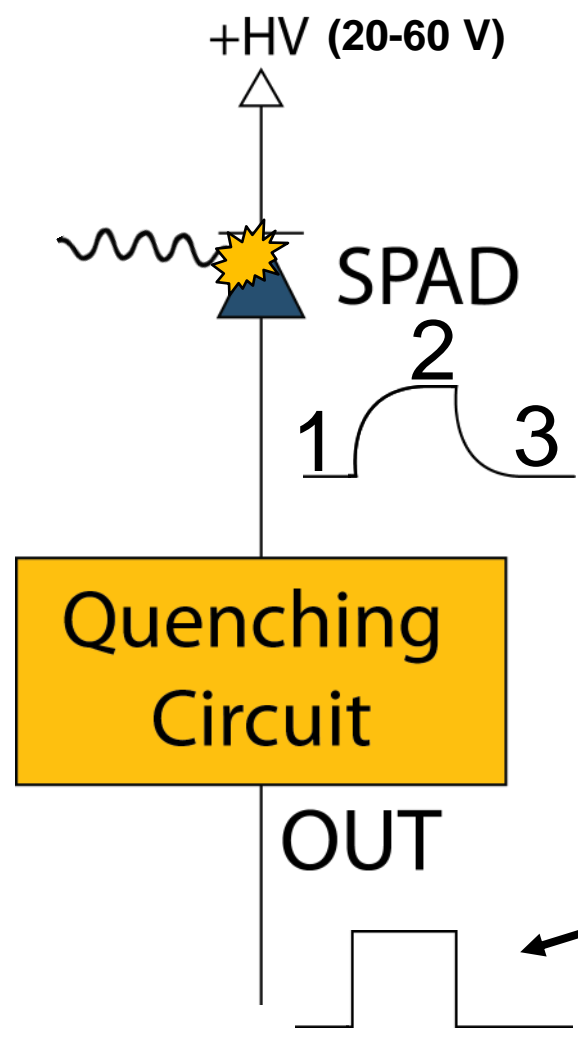


# SINGLE PHOTON AVALANCHE DIODE (SPAD)

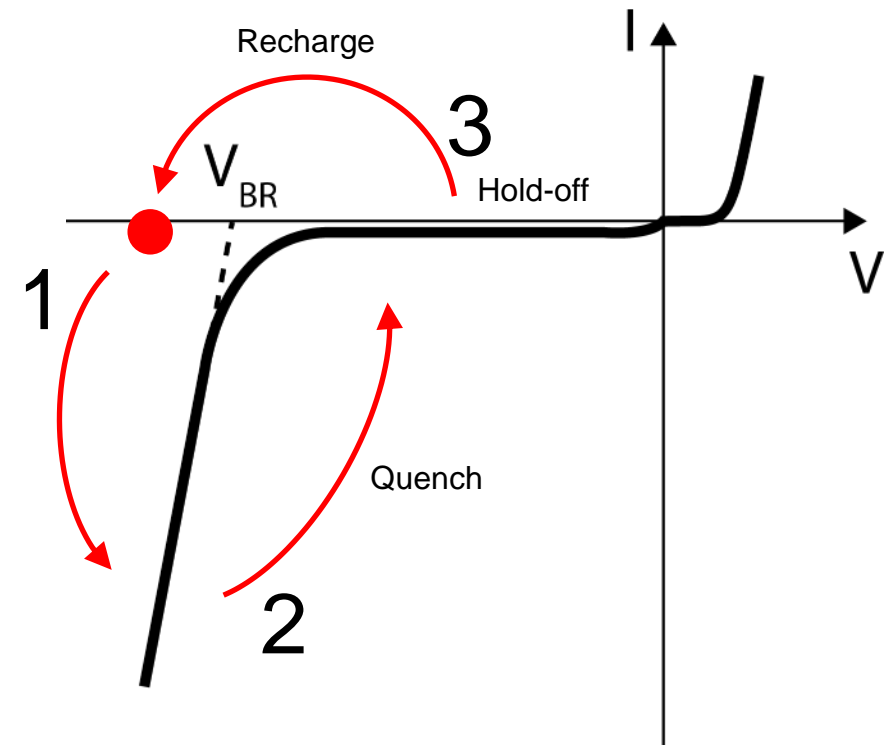
### SPAD cross-section



### Schematic circuit



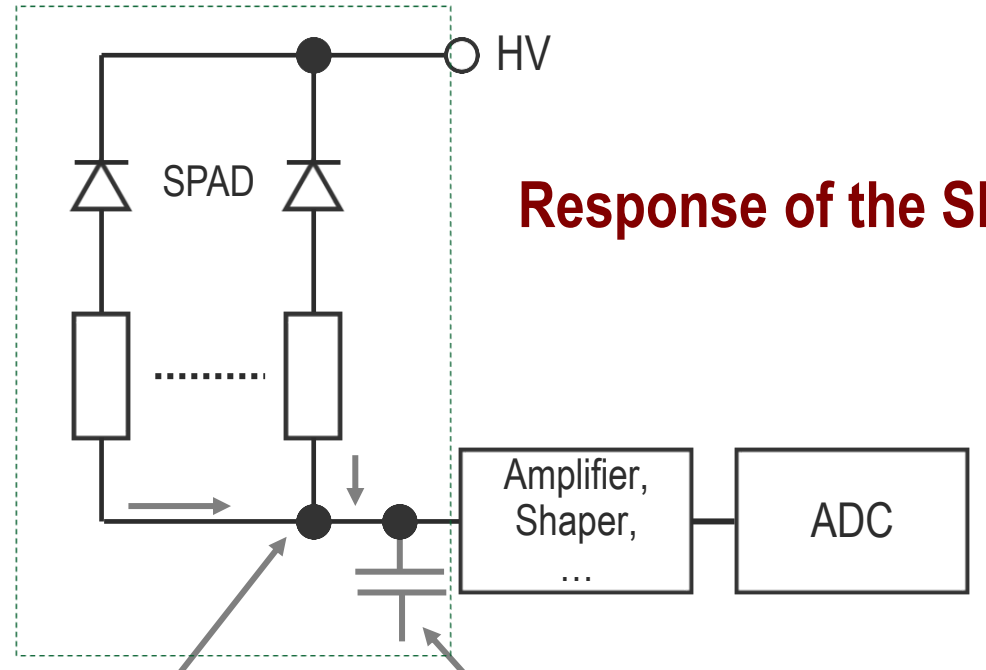
### SPAD I-V curve



**Response of the SPAD is binary**

## SiPM : Silicon Photo Multiplier

Analog SiPM



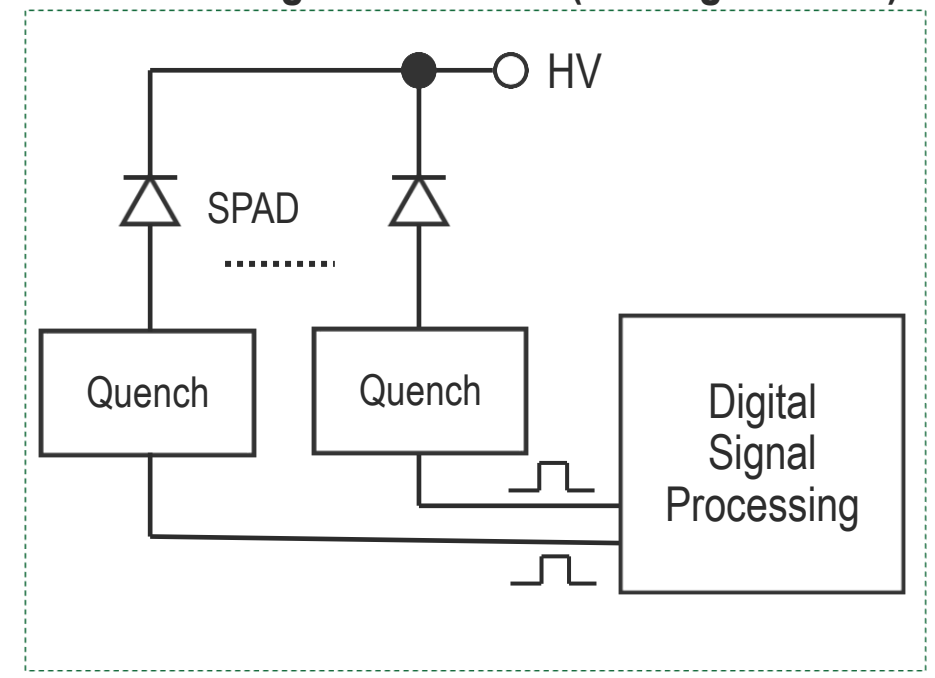
**Response of the SPAD is binary**

Analog current sum

SiPM capacitance → electronic noise

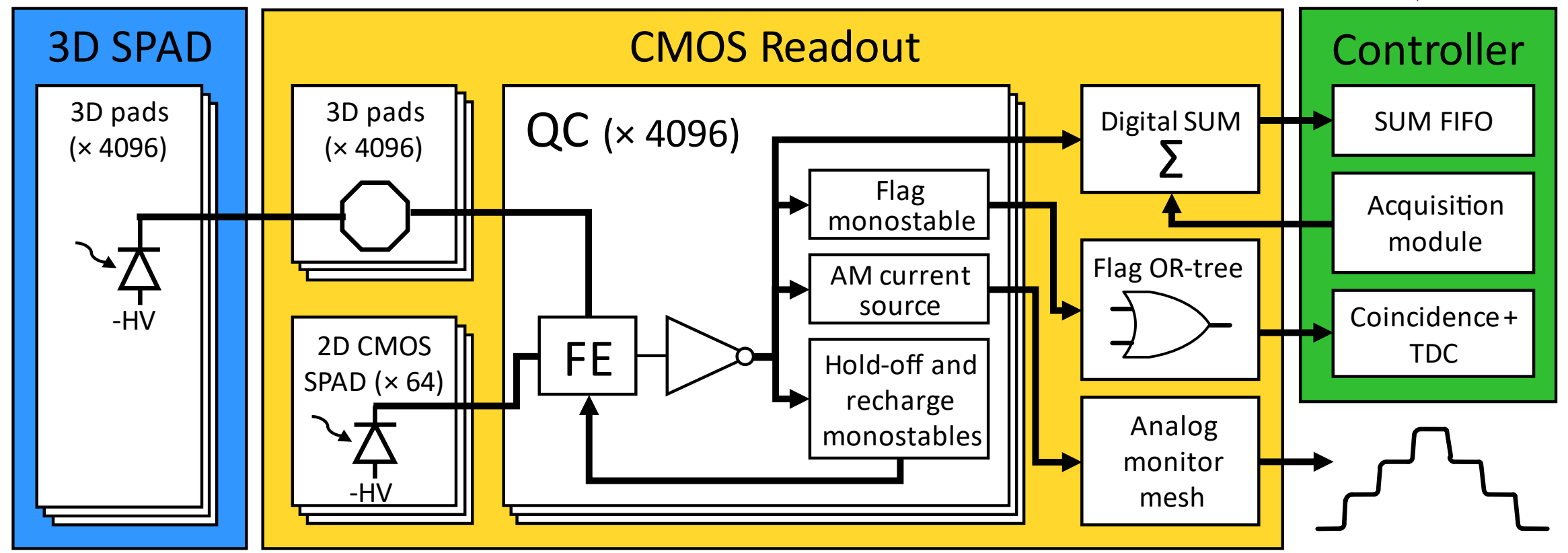
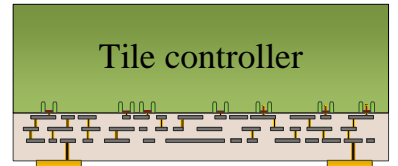
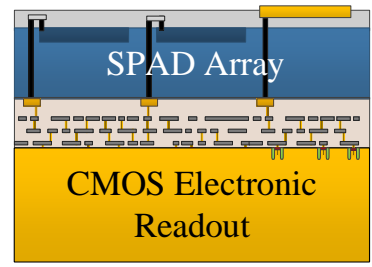
The amplifier transforms charge into voltage and then BACK to digital.

Photon to Digital Converter (aka Digital SiPM)



Individual SPAD readout, no D/A+A/D conversion. Everything stays digital.

# PHOTON-TO-DIGITAL CONVERTER: ARCHITECTURE



## 3D SPAD

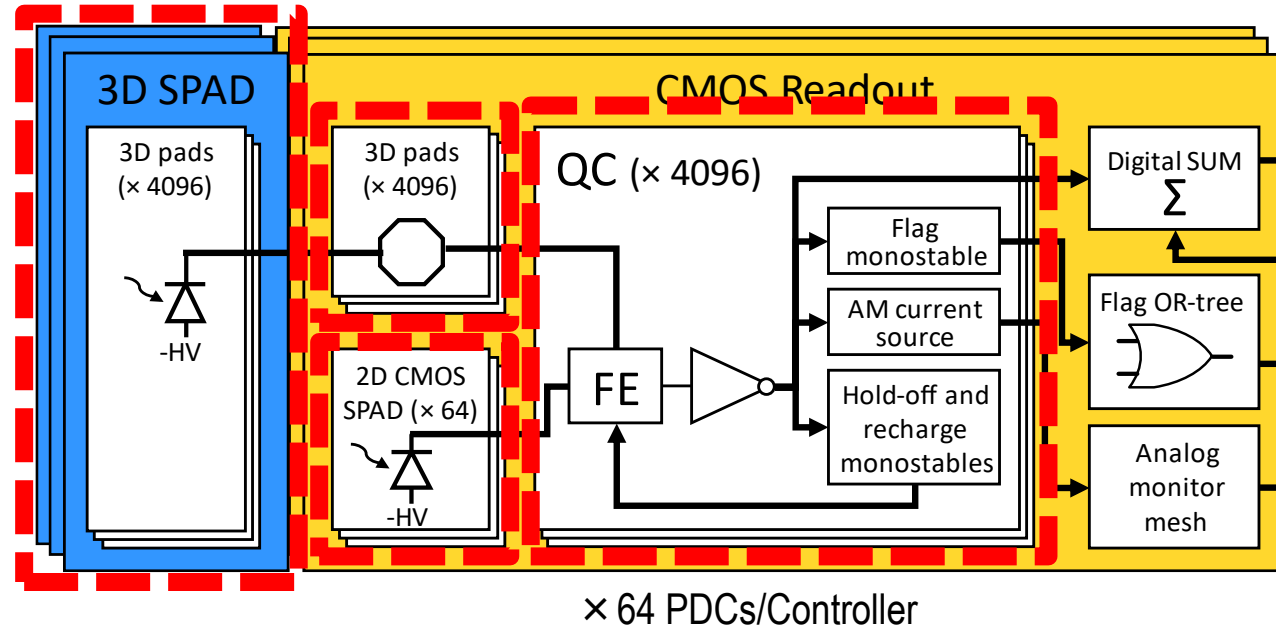
- 4096 SPAD
- 3D pads
- HV at the anode

## CMOS readout pads

- 3D pads (X 4096)
- Individual quenching circuit for each SPAD

## 2D CMOS SPAD

- 64 SPAD on CMOS readout
- Individually quenched



## Quenching circuit

- Read the SPAD from the cathode
- Send the flag
- Hold-off et recharge the SPAD



## Flag output

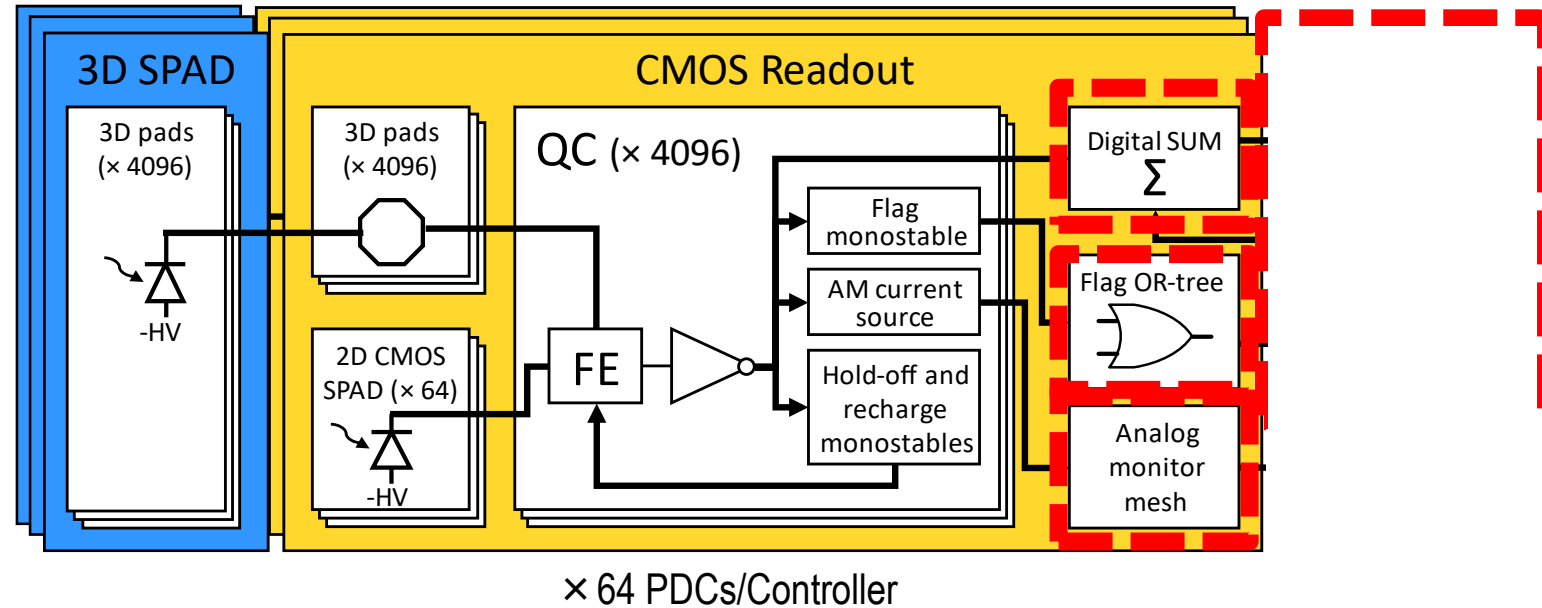
- Pulsed output (adjustable from few ns to tens of ns).
- From an OR-tree.
- Timing jitter better than 100 ps RMS.

## Digital Sum

- Digital count of triggered SPADs inside a bin (dynamic range of 4096 photons).
- Adjustable bin width from 10 ns up to  $\mu$ s.
- Internal FIFO of 128 bins.

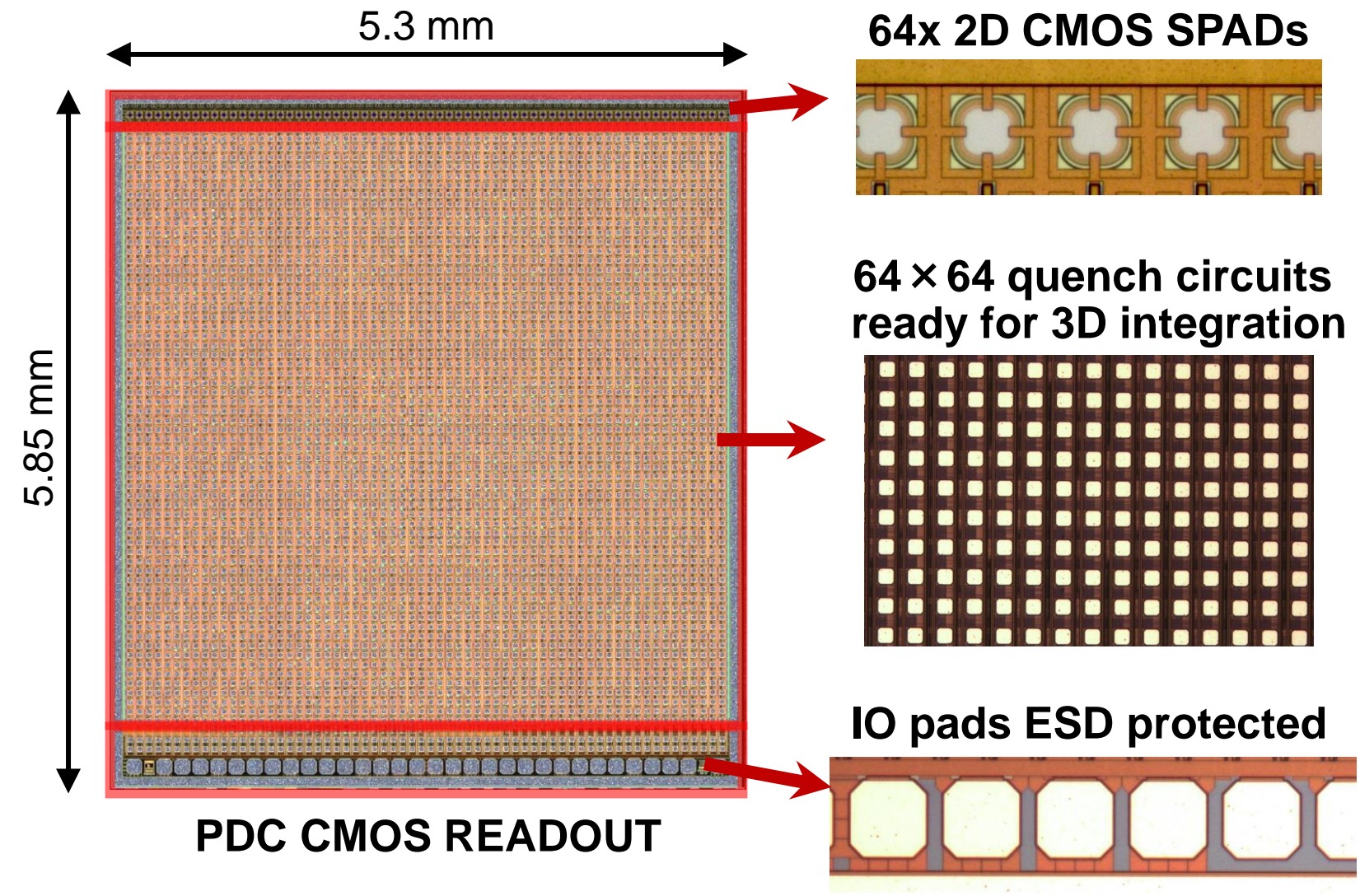
## Analog Monitor

- Current proportional to triggered SPADs.



## Controller (1 for 64 PDCs)

- Start PDC acquisition, based on the number of flag received to discriminate dark count.
- Bank of TDCs for timing measurements on flags.
- Receives data from PDCs and includes post-processing.
- Communicate with an external computer.



## Key Specifications

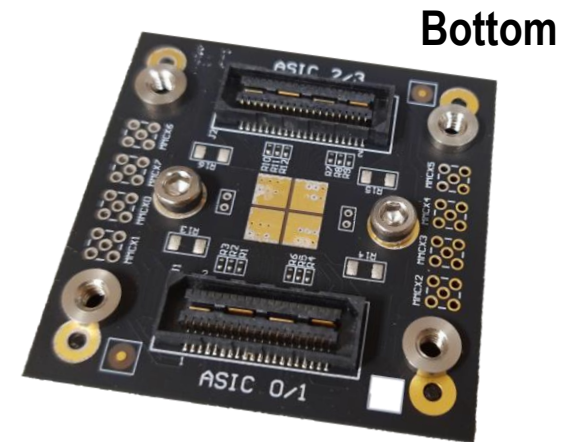
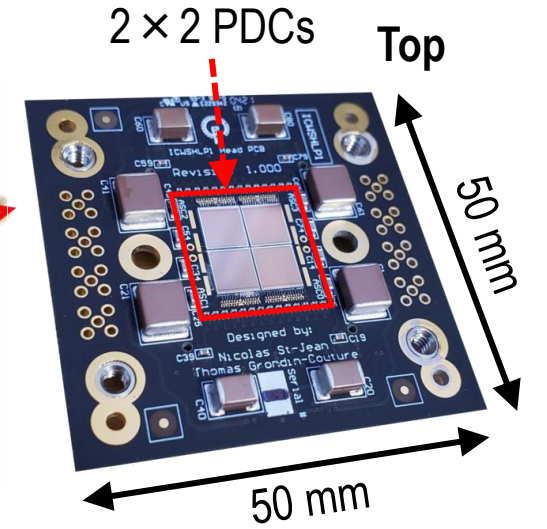
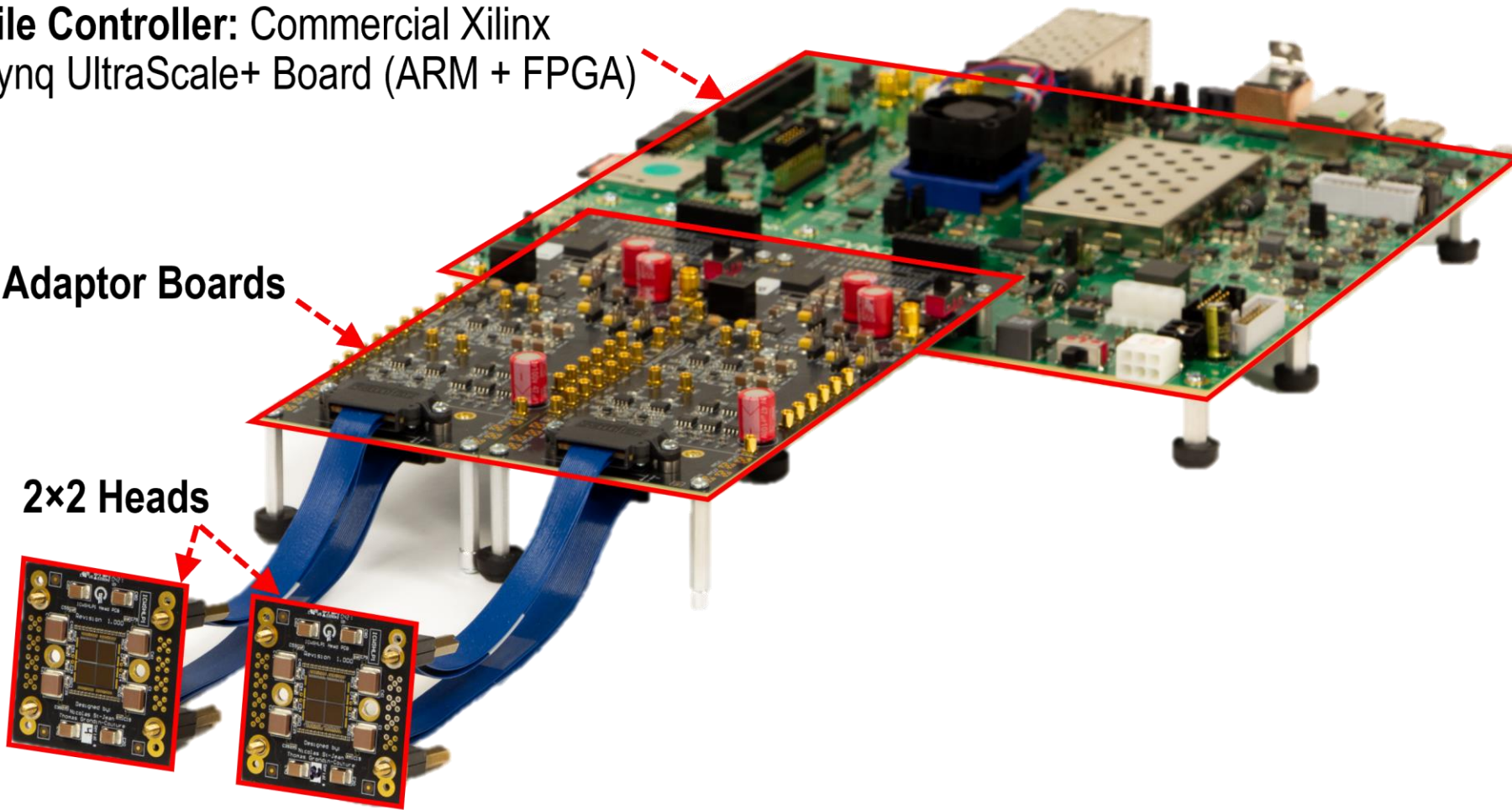
- TSMC 180 nm BCD CMOS process.
- 78  $\mu\text{m}$  SPAD-to-SPAD pitch for a 5X5 mm active area
- Every SPAD is controlled individually.
  - Noisy/defective SPADs can be disabled.
- Dynamic range of 0 to 4096 photons.

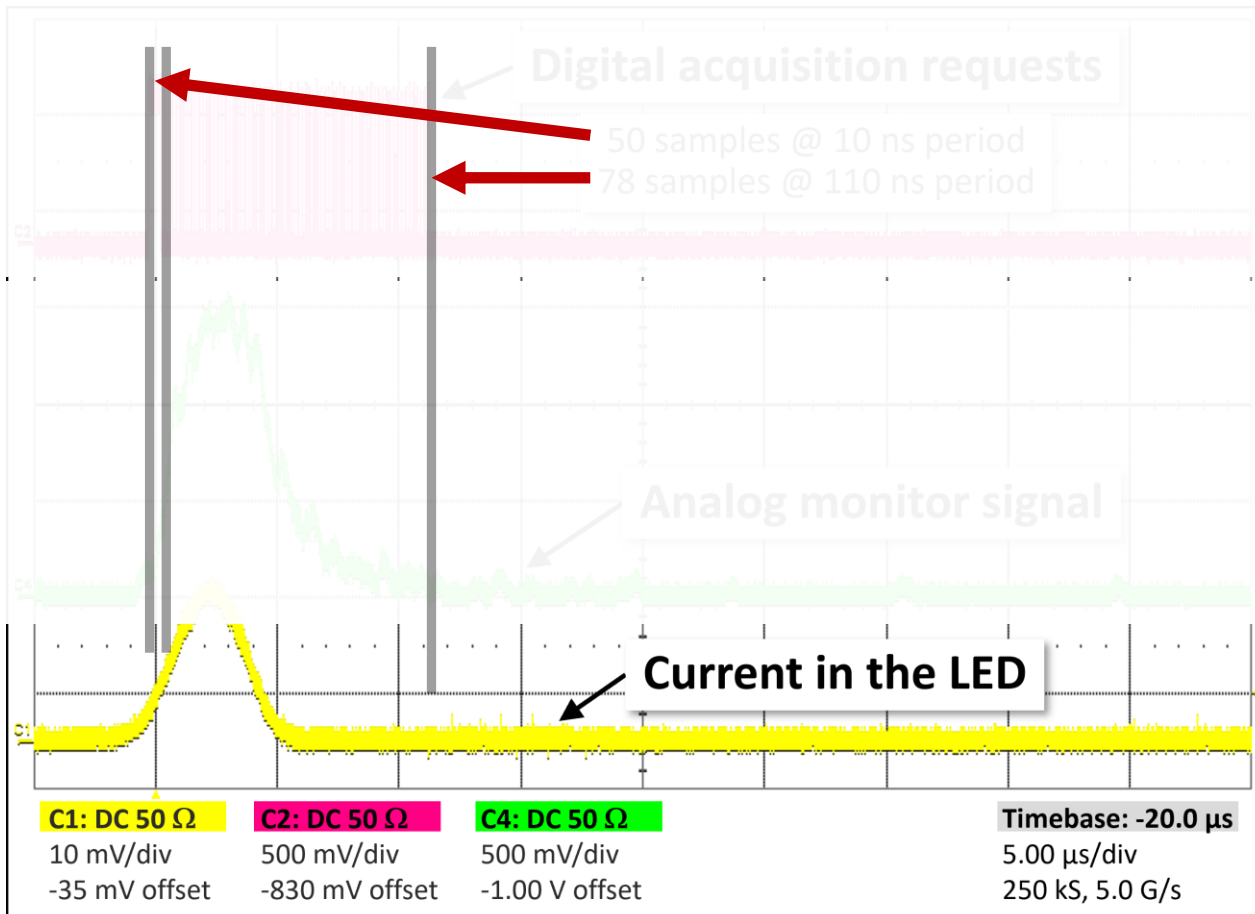
# 2 × 2 PHOTODETECTION MODULE

**Tile Controller:** Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

**Adaptor Boards**

**2x2 Heads**





Using embedded CMOS test SPADs of the PDC

## Current in the LED to trigger the SPADs

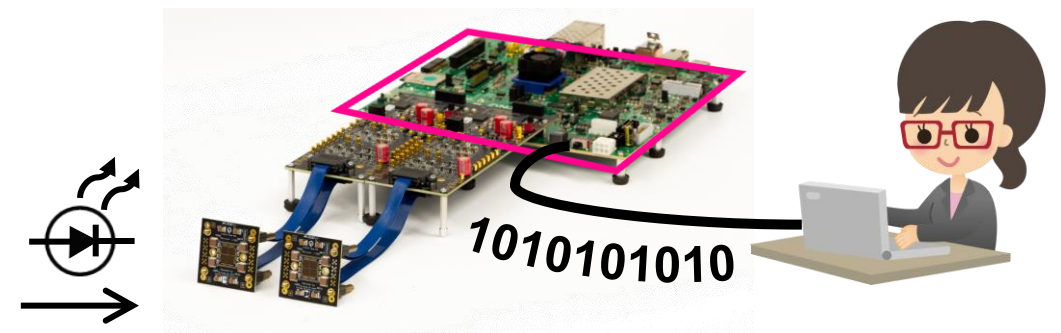
- Driven by a waveform generator

## Analog Monitor

- Amplitude proportional to the number of SPADs triggered

## Digital Sum Acquisition

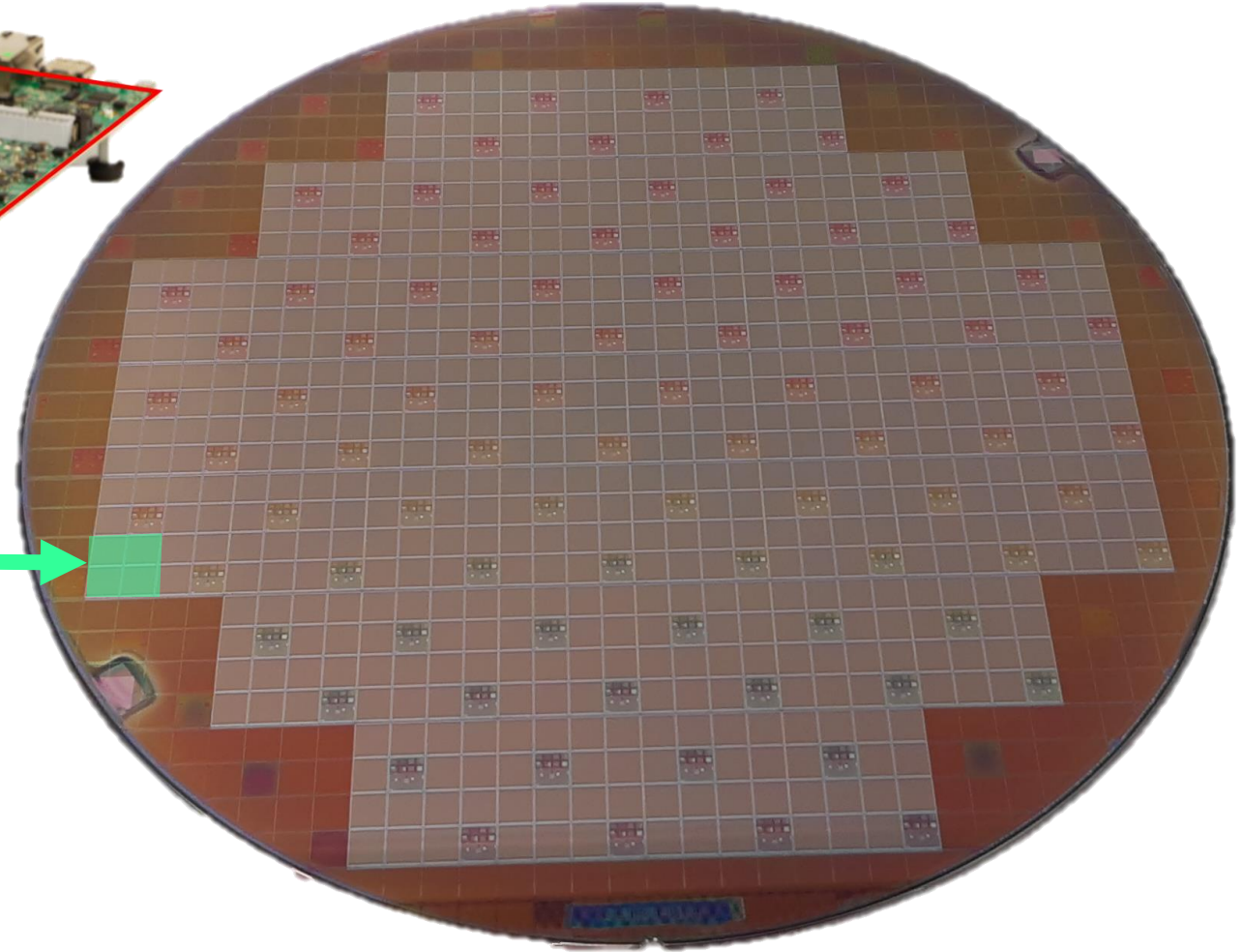
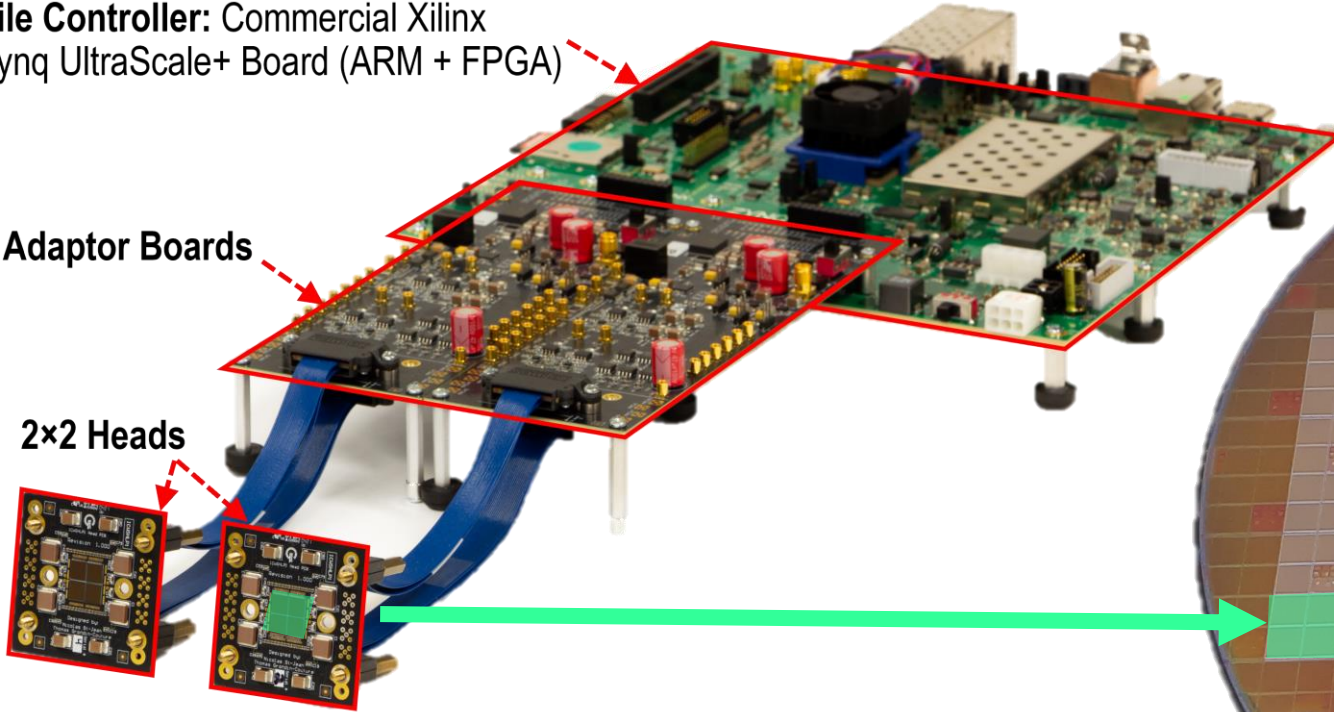
- Based on a 100 MHz readout clock
- Generated by the FPGA (Tile Controller)



**Tile Controller:** Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

**Adaptor Boards**

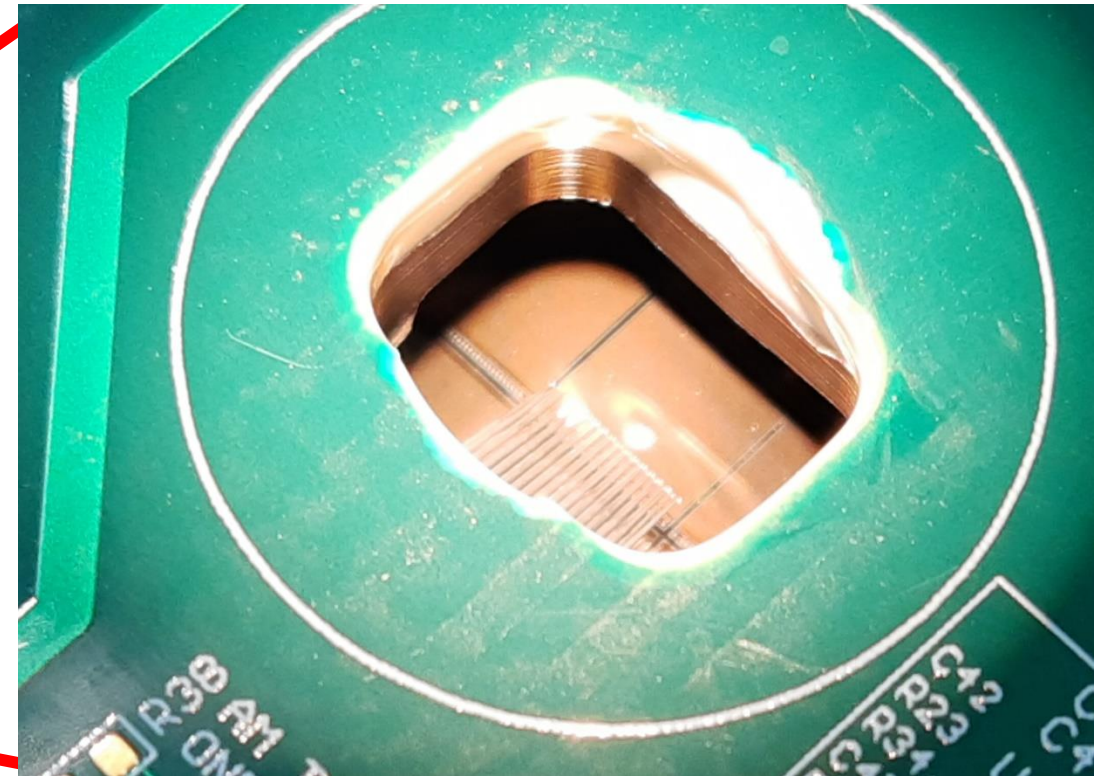
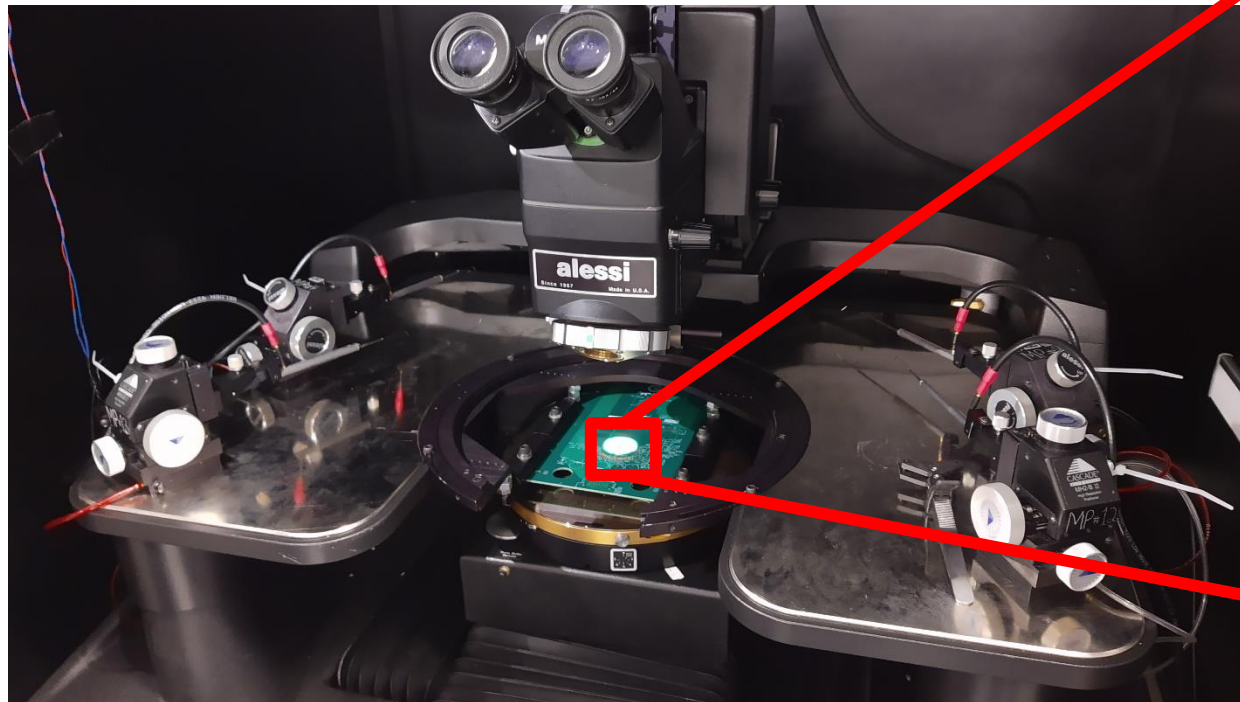
**2x2 Heads**



**200 mm wafer of PDCs**

## Dedicated probe card

- Active probe card with FPGA
- Passive probe card

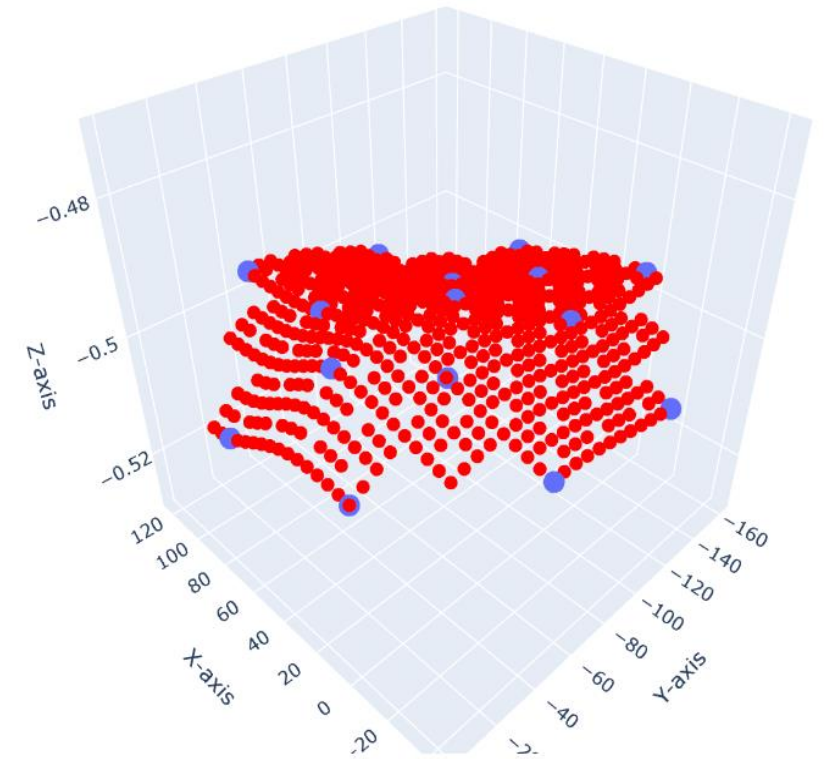
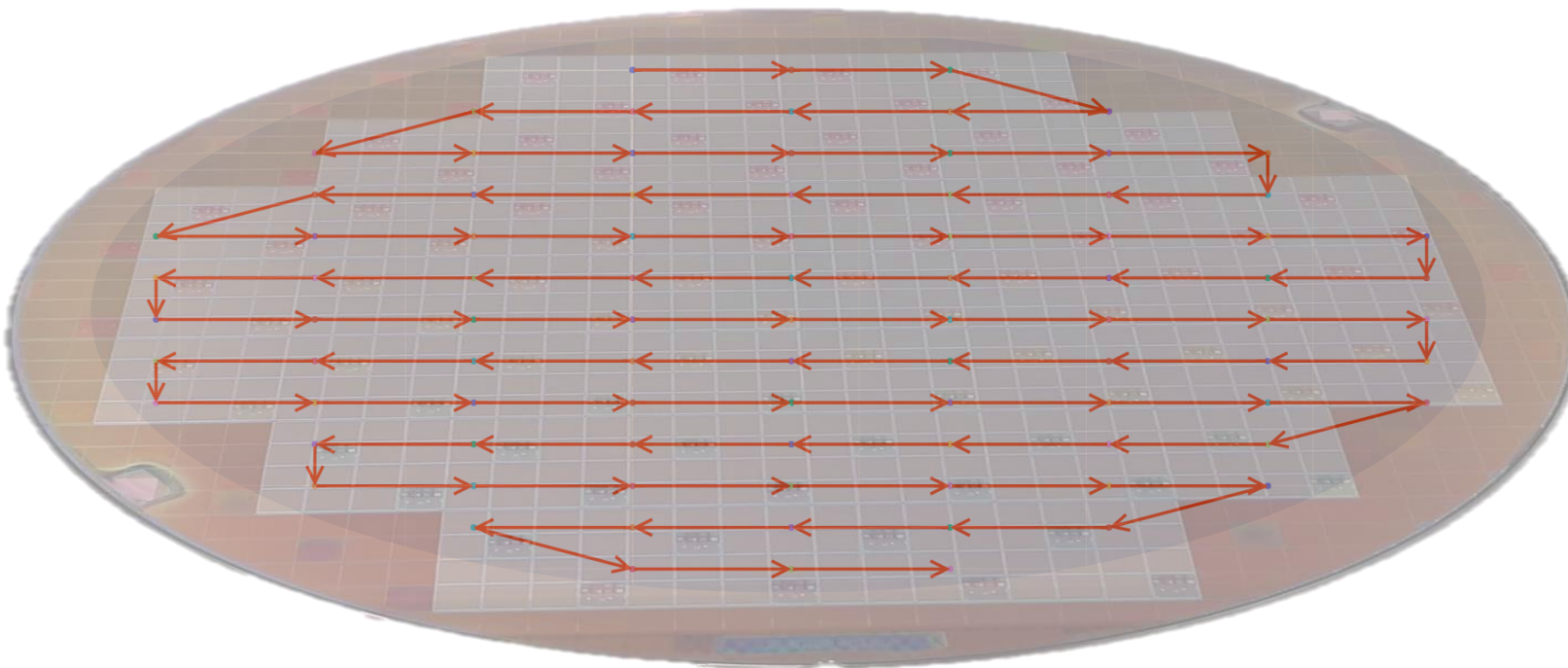


Needles of the probe card

Probe station with probe card attach to it

Automated movement for wafer-level measurement (over 600 PDC)

Adjusting the height of contact according to wafer topology



Movement of the chuck in relation to the wafer

Wafer topology

- Photon-to-Digital Converters keep the information digital all along the acquisition chain.
- FPGA-based tile controller gives a lot of flexibility to implement multiple features.
  - Flag-based acquisition, dark count mitigation, pulse shape discrimination, and so on.
- Tile Controller ASIC in development to replace the FPGA boards.
- Wafer level measurement will accelerate the testing of multiple PDC for larger system integration.



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Fonds de recherche  
sur la nature  
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- [1] nEXO Collaboration *et al*, “Nexo Pre-Conceptual Design Report,” *arXiv.org*, 13-Aug-2018. [Online]. Available: <https://arxiv.org/abs/1805.11142>.
- [1] M. R. Heath *et al.*, “Development of a Portable Pixelated Fast-Neutron Imaging Panel”, DOI:[10.1109/TNS.2021.3136344](https://doi.org/10.1109/TNS.2021.3136344).



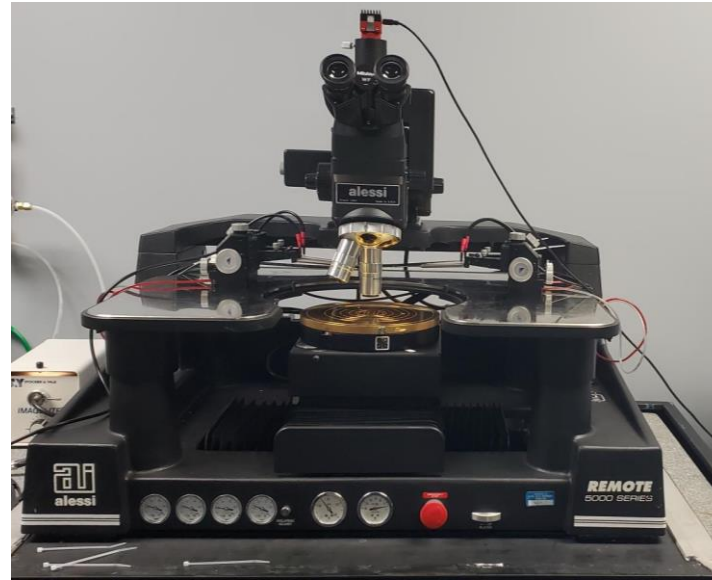
# BACKUP

## Probe station

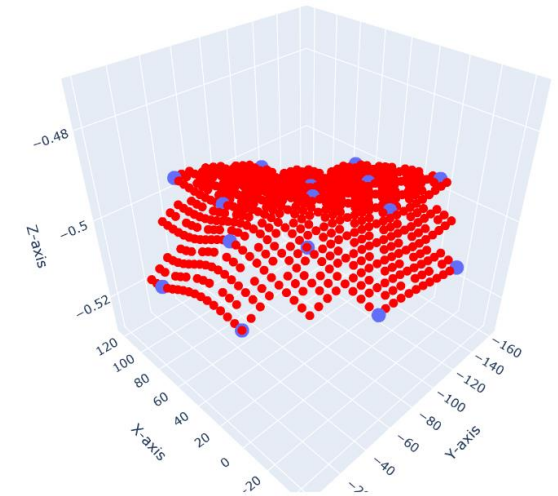
- Fully automatic chuck enabling scripts for multiple measurement on a wafer
- Program to adapt for the wafer topology

## Probe card

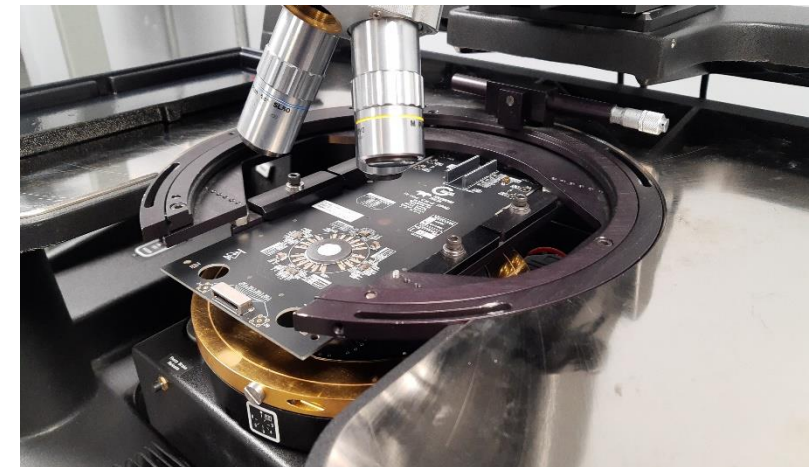
- Can act as the interface between the PDC and the controller (FPGA)



Probe station

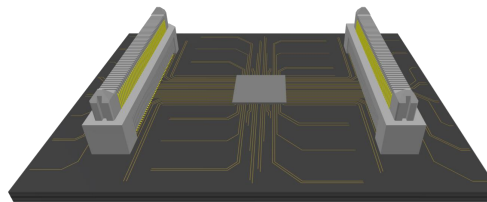
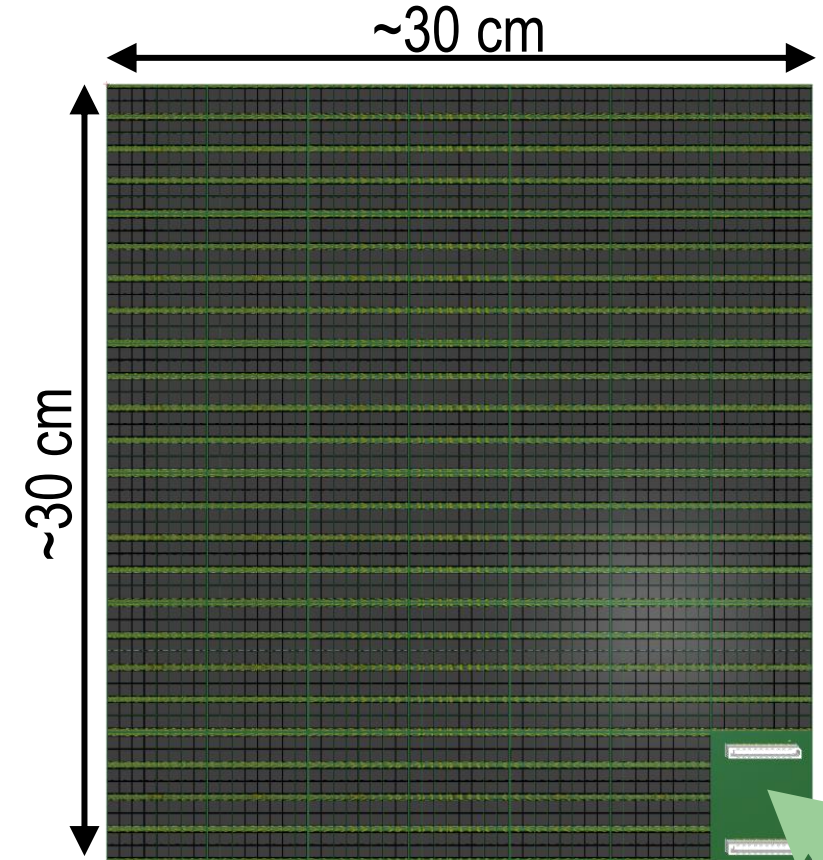


Wafer topology

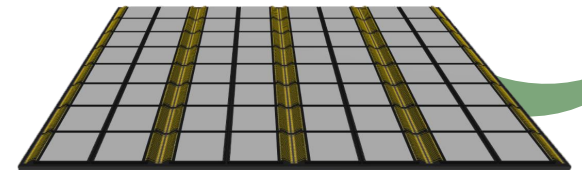


Probe card on the station

- PDC panel array of 42 modules of 8 x 8 PDC
- 400-500 nm peak pixelated plastic scintillators
- 11E+6 SPADs over 30 x 30 cm<sup>2</sup>
- 40W PDC power consumption
  - 10 ns binning for 3k events/s/PDC,
  - 128 bins/event (1280 ns range/event)
- Simulated timing distribution PDC of 25 ps RMS

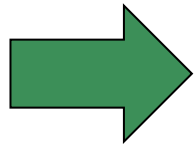
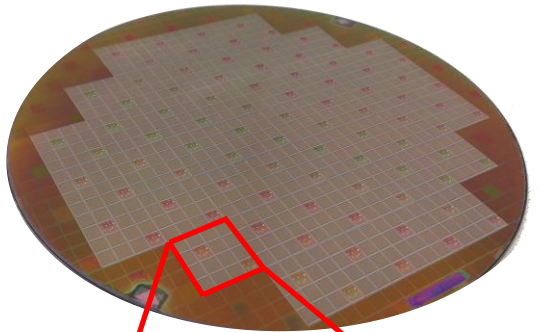


**Bottom side**

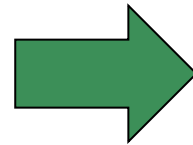
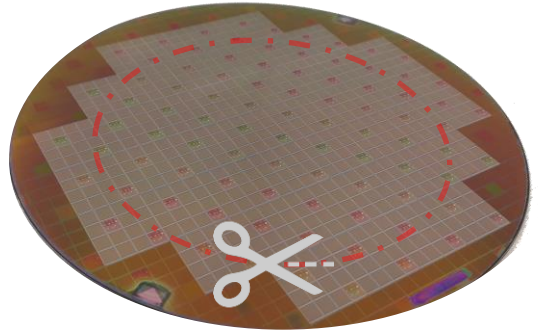


**Top side**

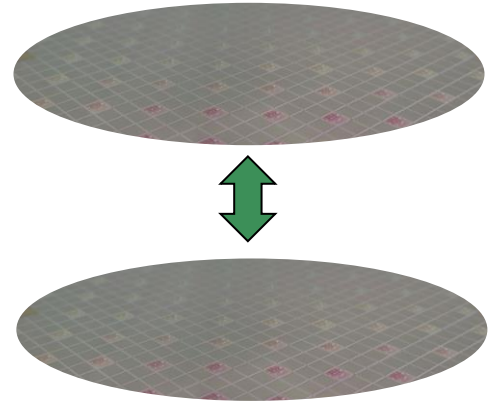
8 inch CMOS wafer



8 inch to 6 inch coring down



3D Bonding @ Teledyne DALSA (TDSI)



6 inch SPAD wafer

6 inch CMOS wafer

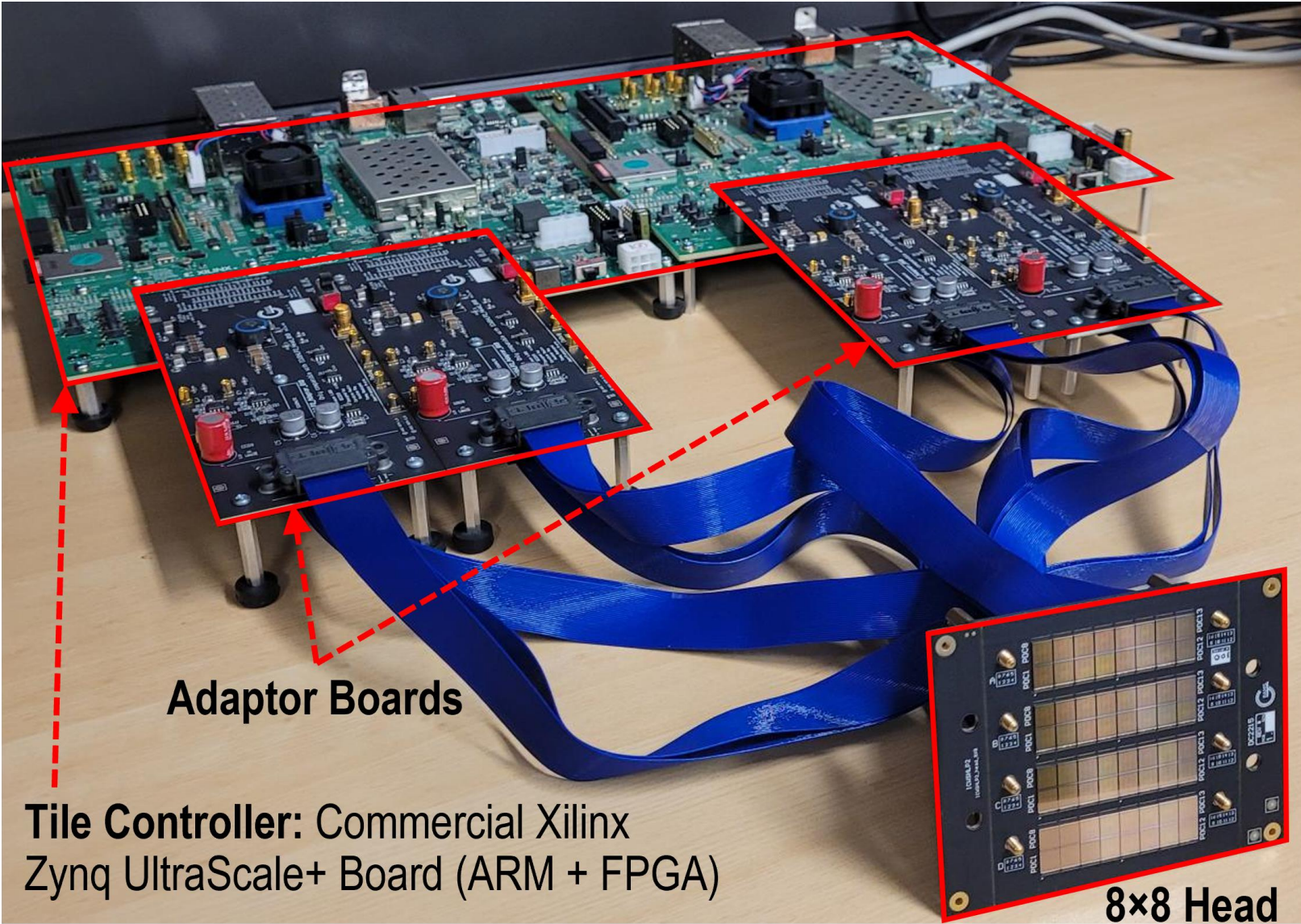
Alignment die for 3D bonding

PDC CMOS readout

Reticle of 4 x 4 dies

\*SPAD process & 3D bonding process completed @ TDSI

# 8 × 8 PHOTODETECTION MODULE

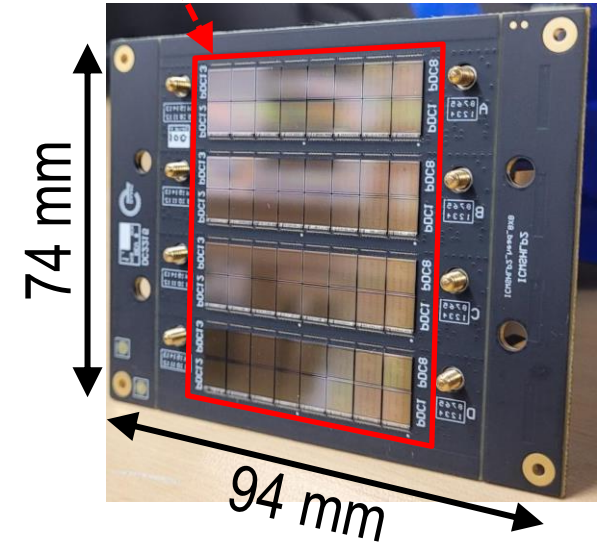


**Tile Controller:** Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

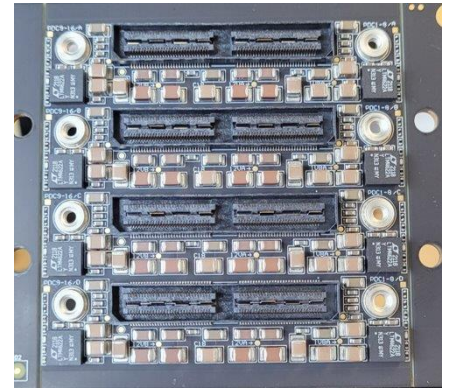
**Adaptor Boards**

**8x8 Head**

**8 × 8 PDCs**



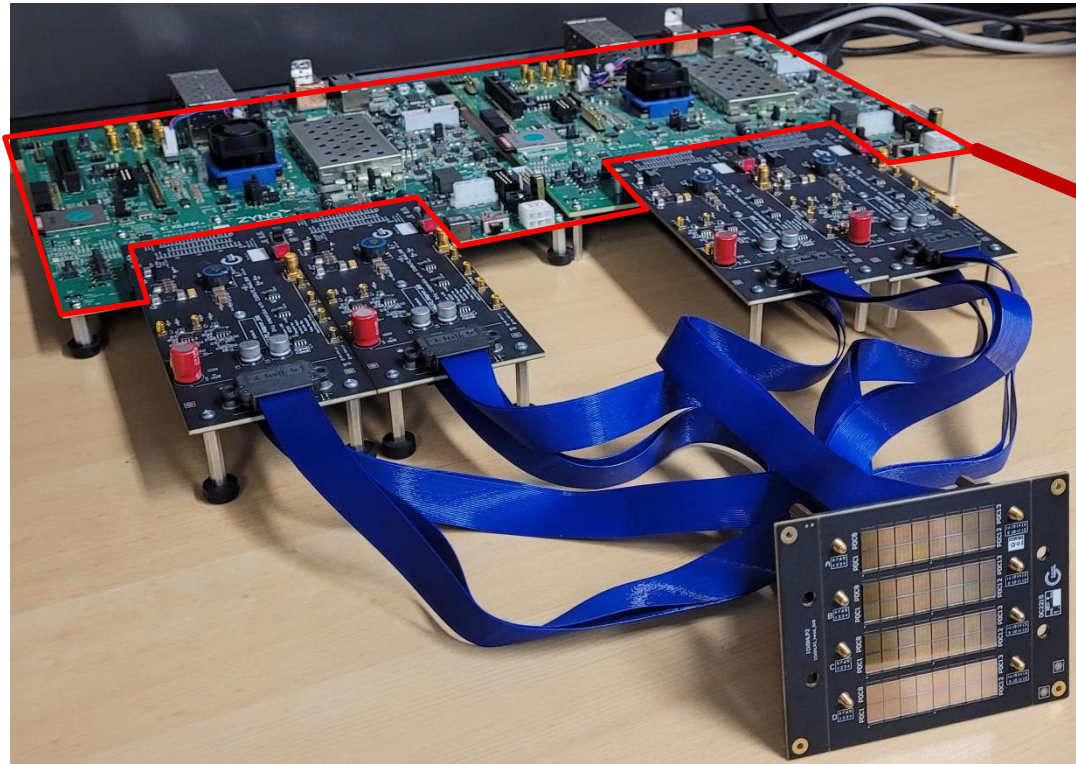
**Top**



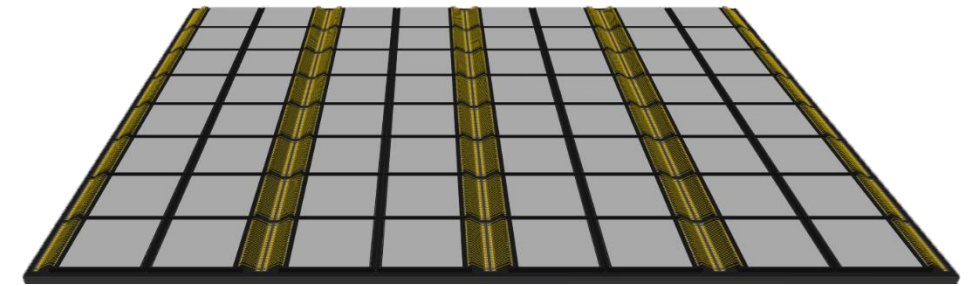
**Bottom**

**8 × 8 PCB tile prototype**

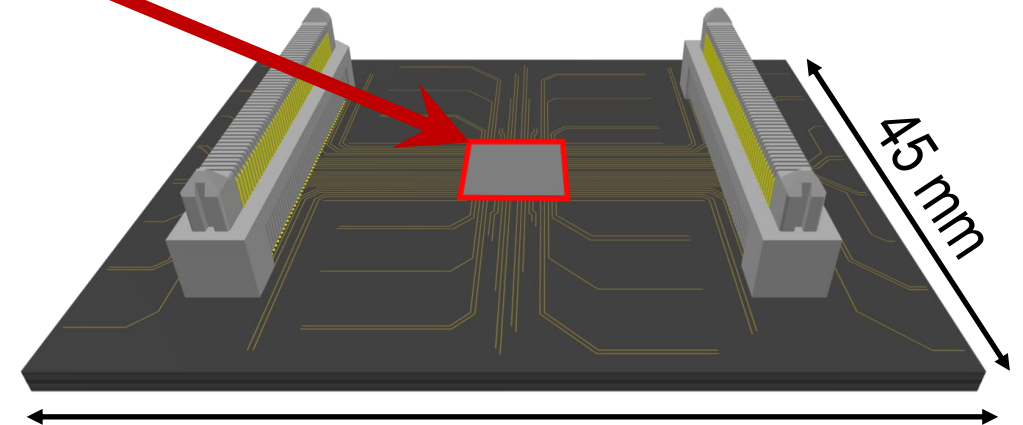
## FPGA-based Controller



## ASIC-based Controller



Top side



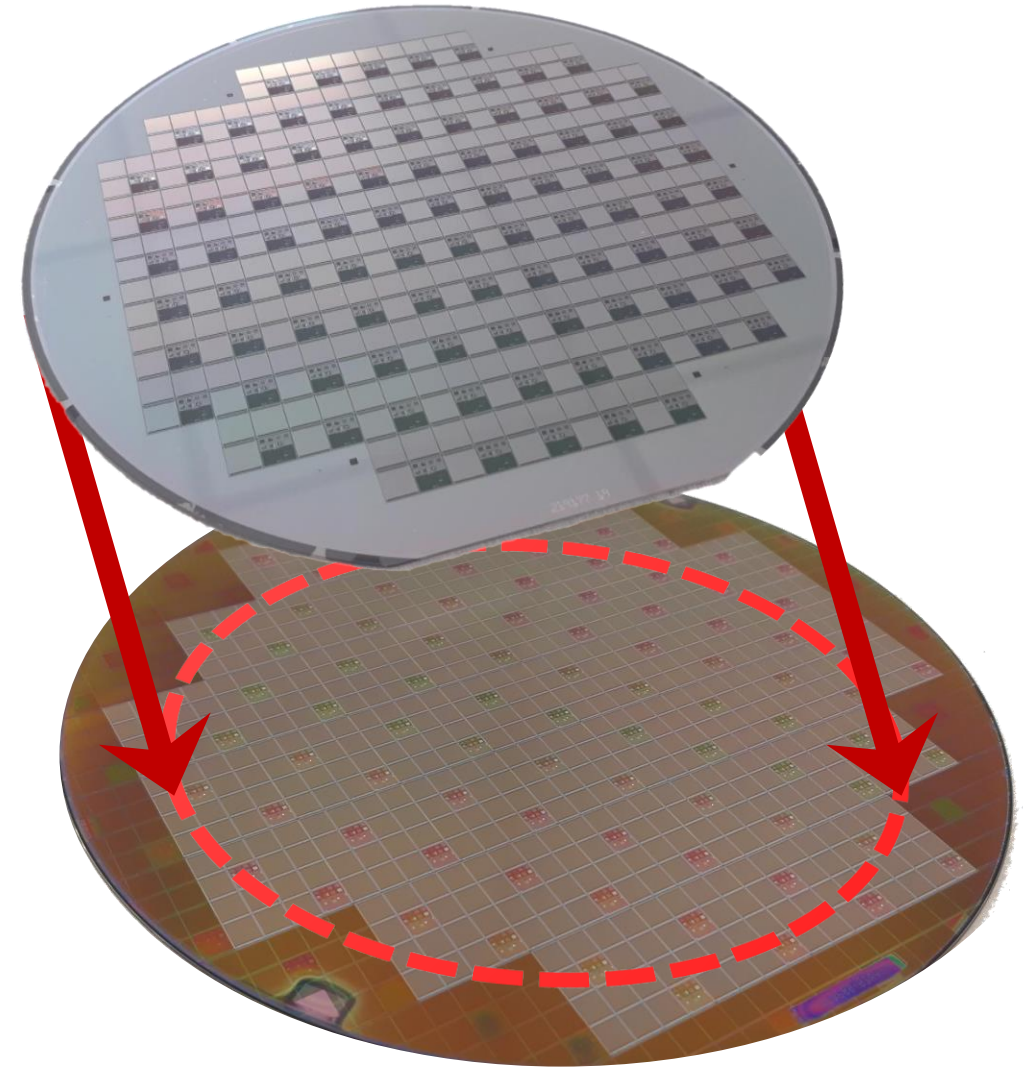
57 mm

45 mm

Bottom side



**150 mm SPAD wafer**



**200 mm PDC wafer**