#133

PHOTON-TO-DIGITAL CONVERTER FOR LARGE SCALE NOBLE LIQUID DETECTORS AND NEUTRON IMAGING

Olivier Lepage[1,2], Tommy Rossignol[1,2], Nicolas Roy[1,2], Frédéric Vachon[1,2], Keven Deslandes[1,2], Arnaud Samson[1,2], Lorenzo Fabris[3], Jean-François Pratte[1,2] and Serge A. Charlebois[1,2]

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[2] Interdisciplinary Institute for Technological Innovation, Sherbrooke, Québec, Canada
[3] Oak Ridge National Laboratory, Oak Ridge, United States

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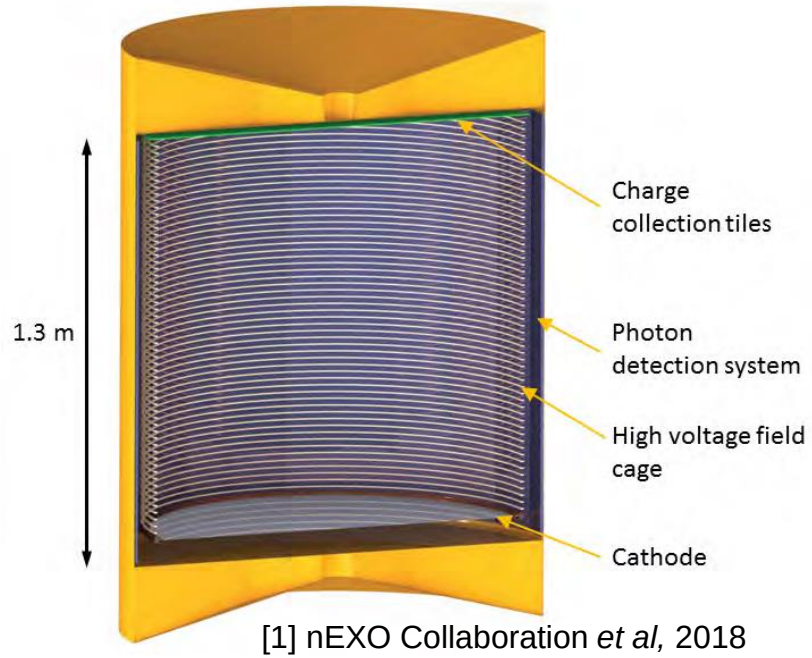
61st Winter Nuclear & Particle Physics Conference

OAK RIDGE National Laboratory

UdS Université de Sherbrooke

Large Scale Noble Liquid Experiments

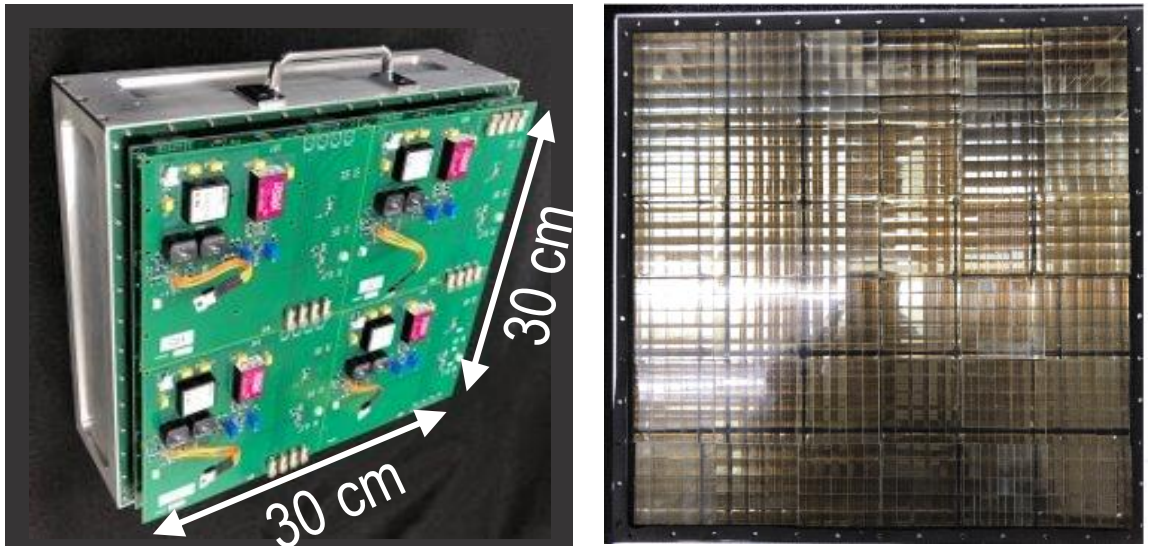
- Neutrinoless double beta decay and dark matter search
- 4.6 m^2 of detectors
- 200 W max.



[1] nEXO Collaboration *et al,* 2018

Neutron imaging

- Large pixelated sensitive area
- Portability (compact and low-power)



ORNL Portable Pixelated Fast-Neutron Imaging Panel [2]

Large Scale Noble Liquid Experiments and Neutron Imaging

Large Scale Noble Liquid Experiments

- Neutrinoless double beta decay and dark matter search
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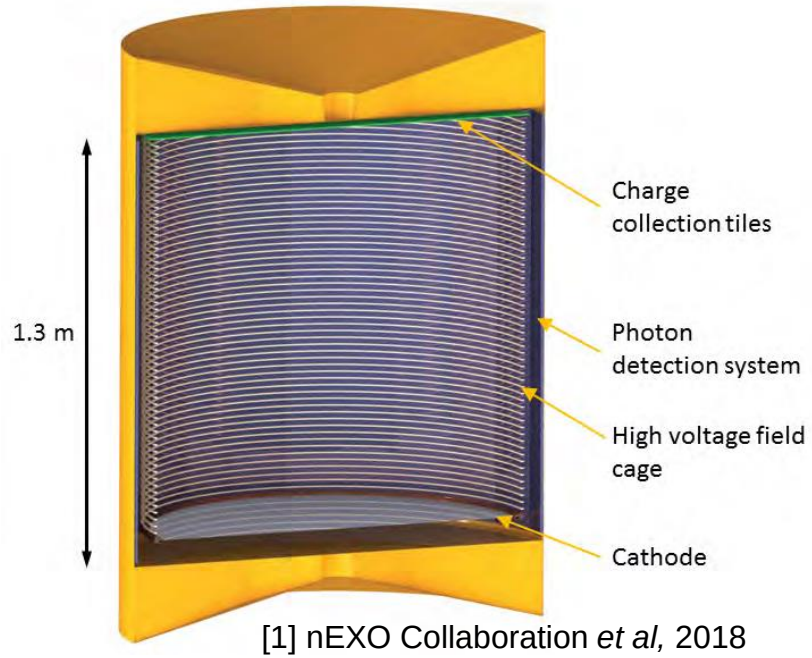

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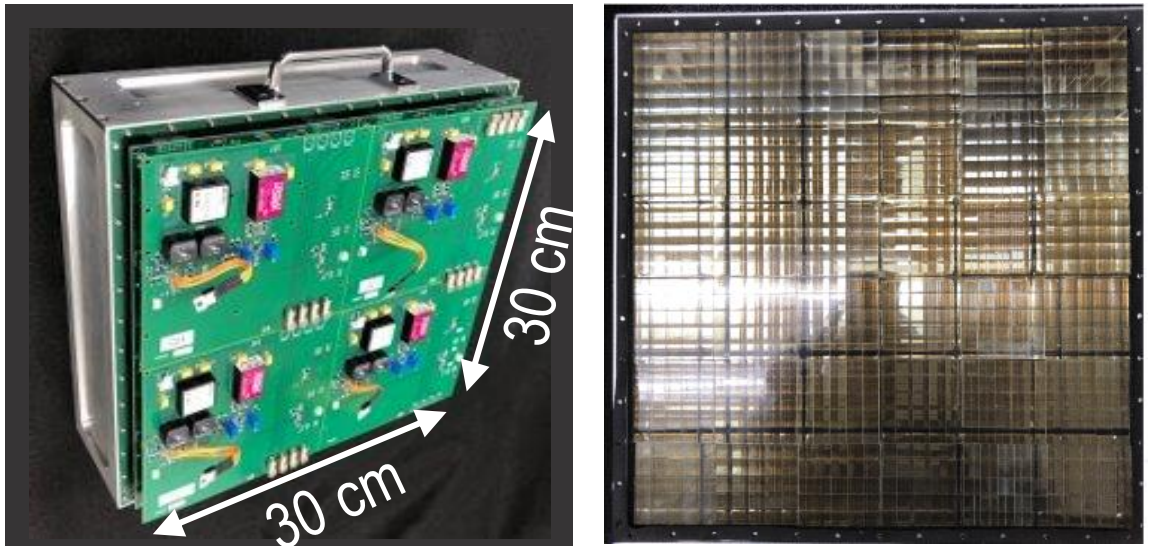
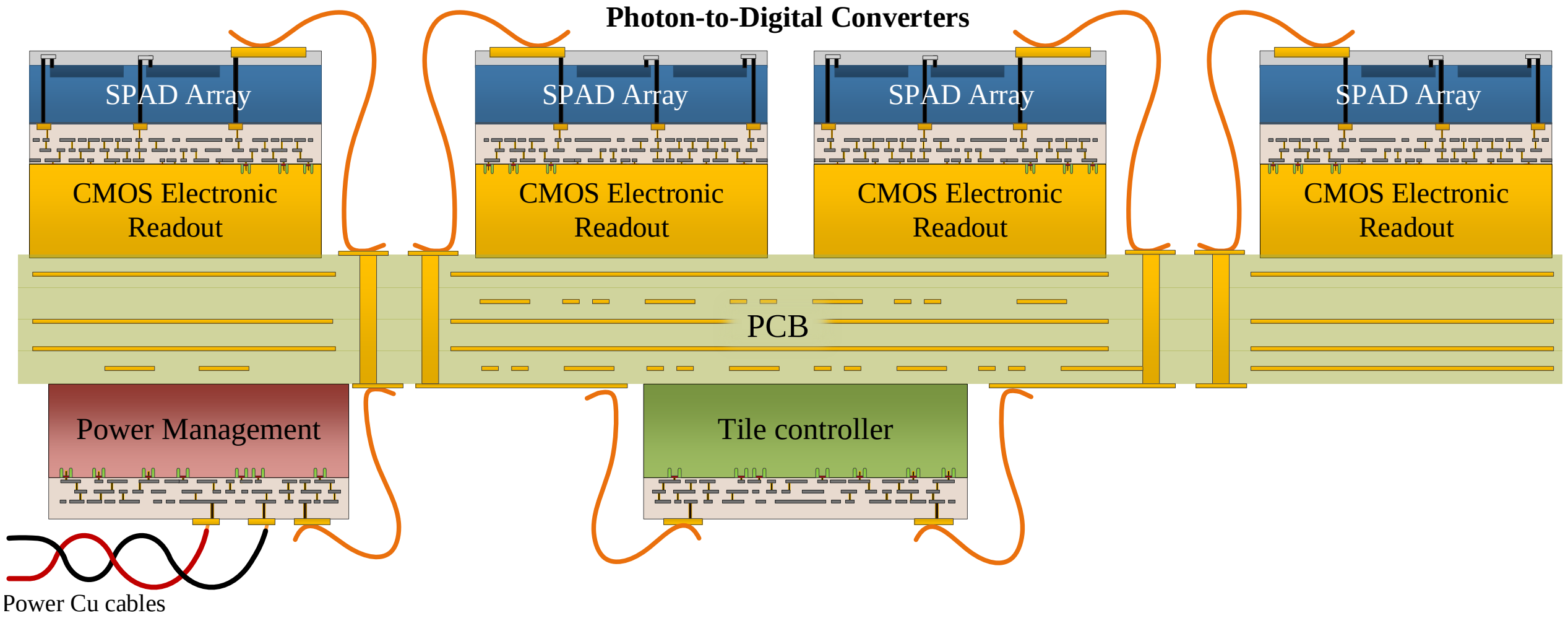


ORNL Portable Pixelated Fast-Neutron Imaging Panel [2]

Need : Large area, low-power and good timing precision photon counting system.

DIGITAL SOLUTION: 3DPDC + TILE CONTROLLER



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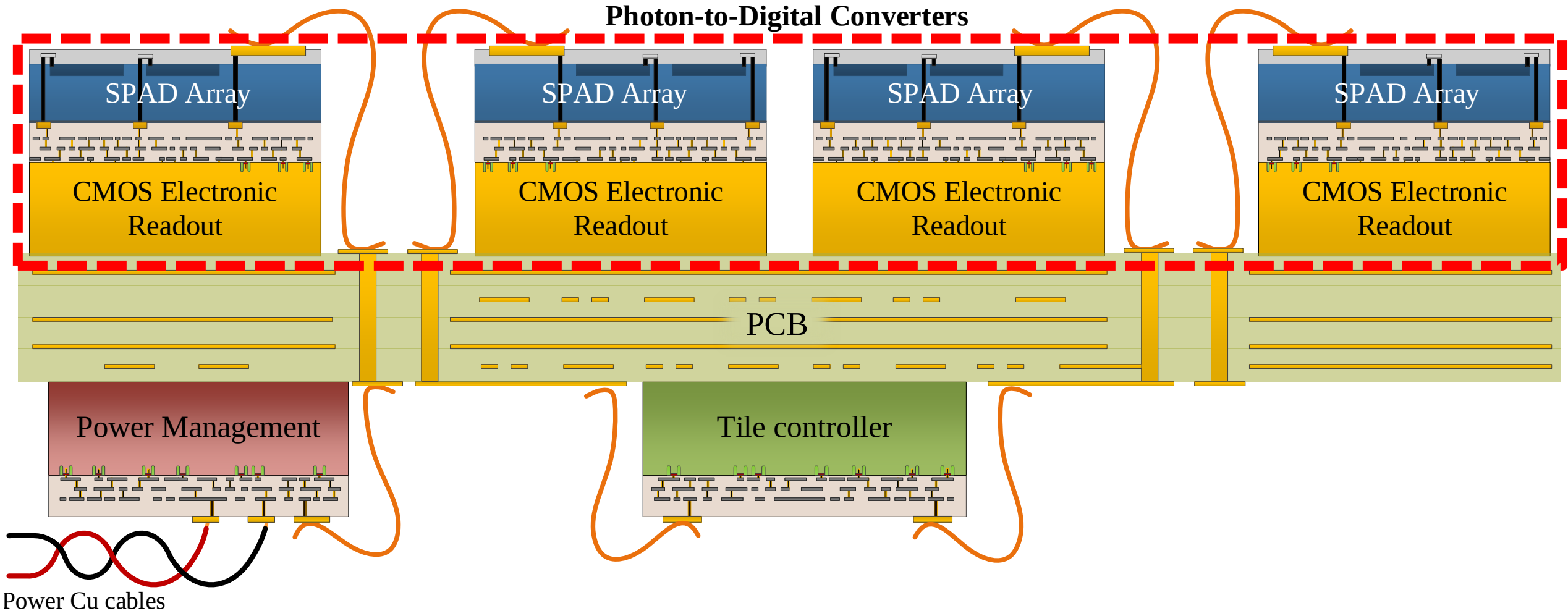

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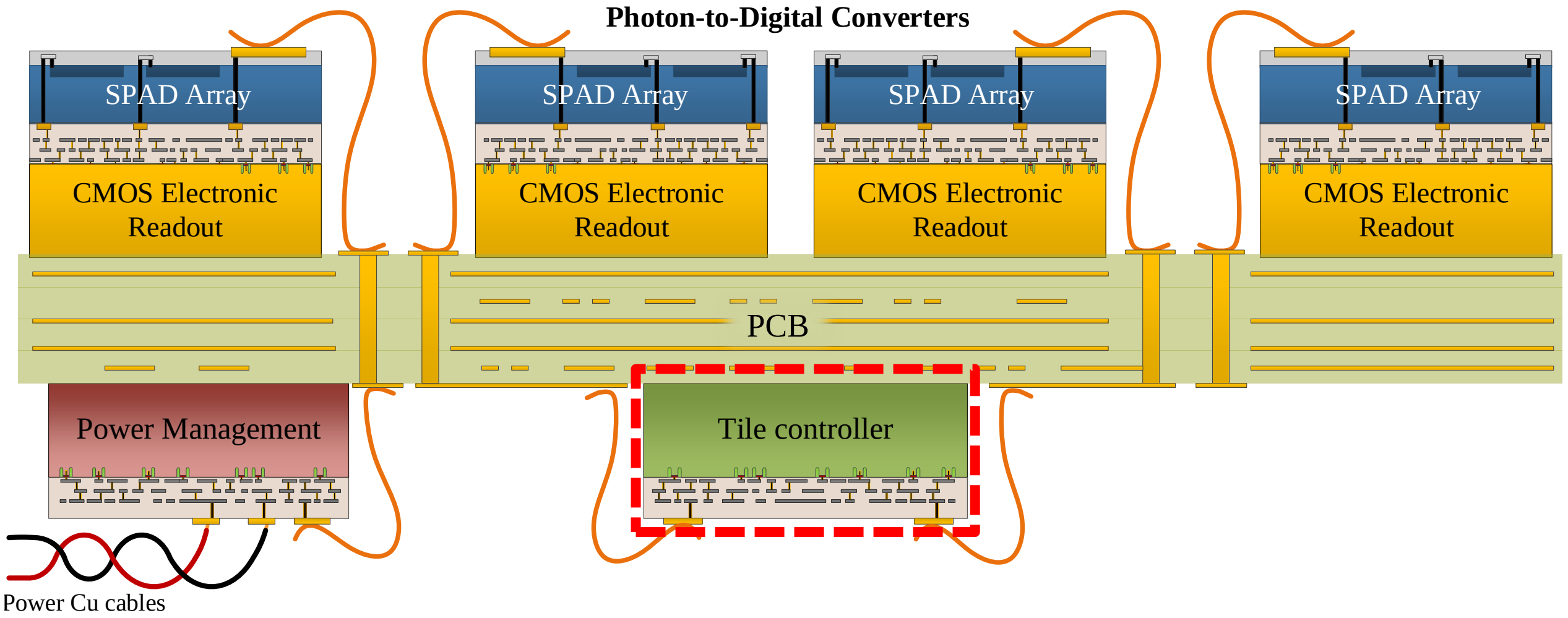

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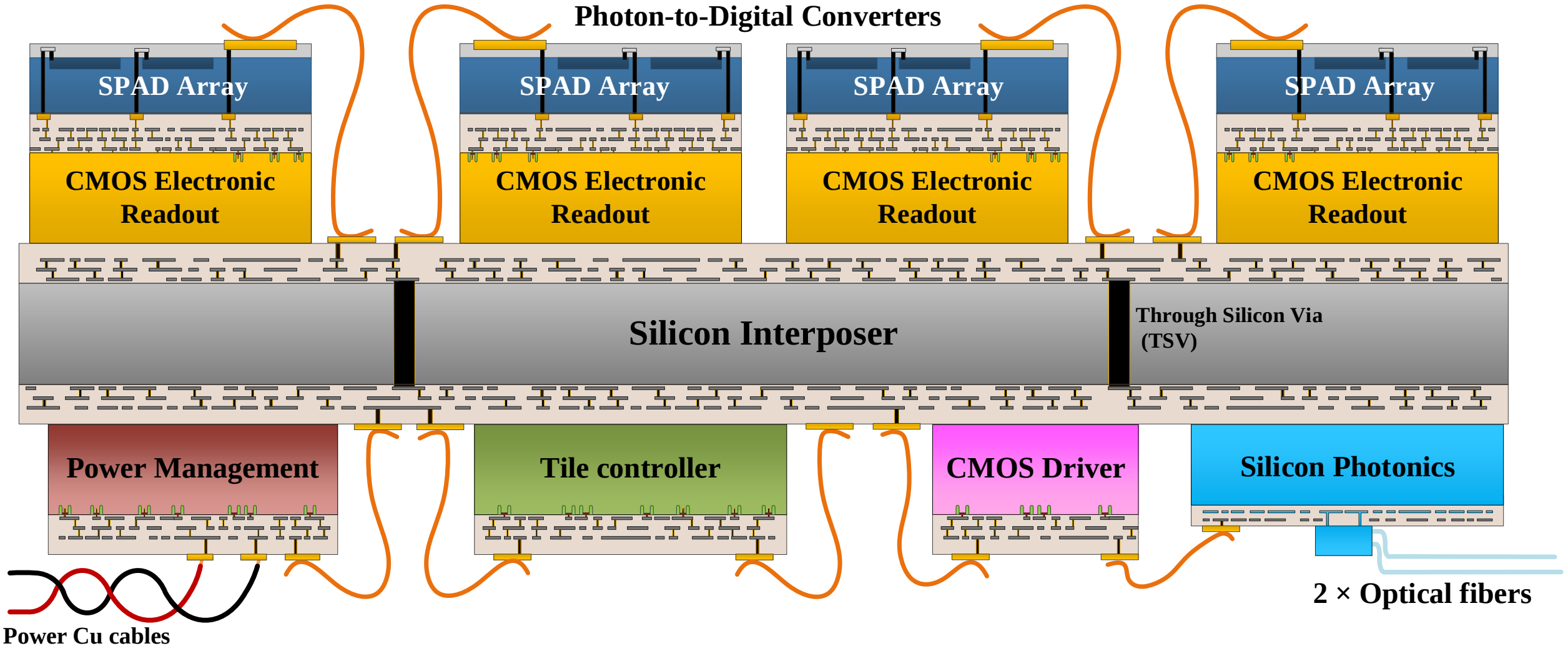

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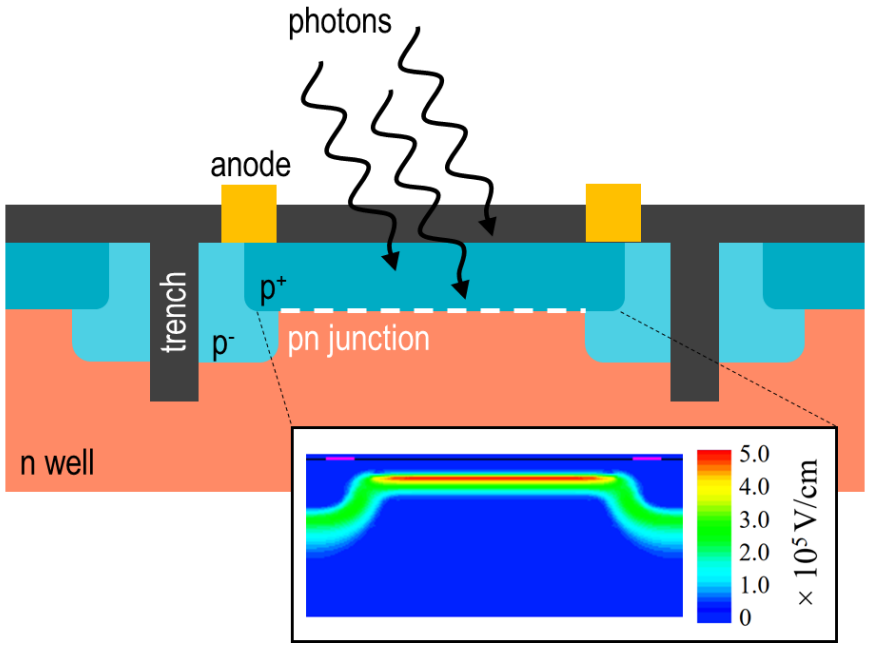
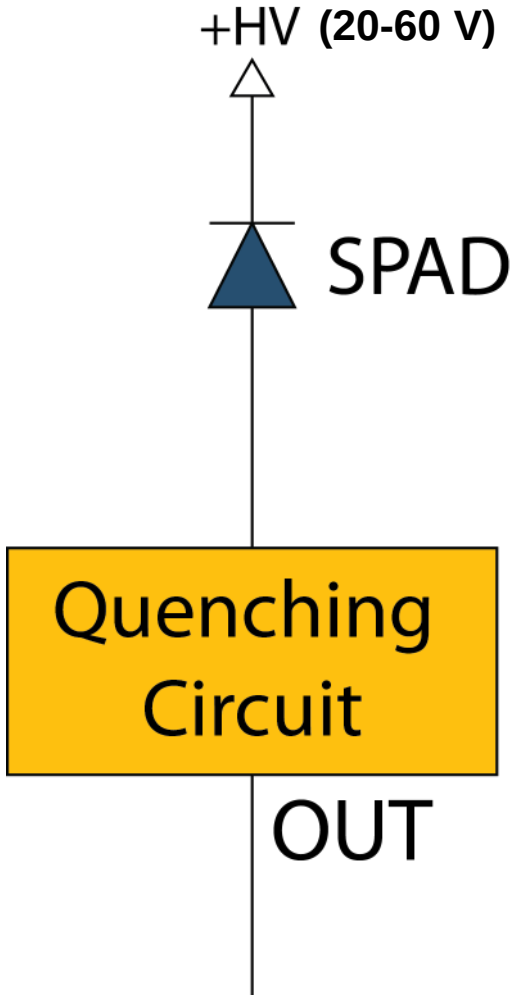
SINGLE PHOTON AVALANCHE DIODE (SPAD)

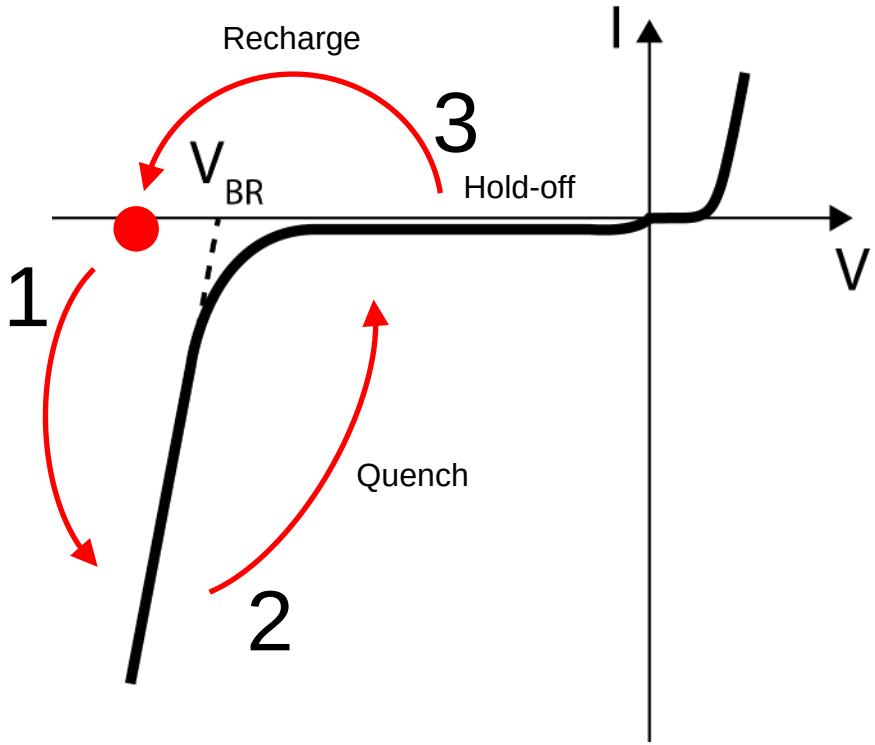
SPAD cross-section



Schematic circuit



SPAD I-V curve



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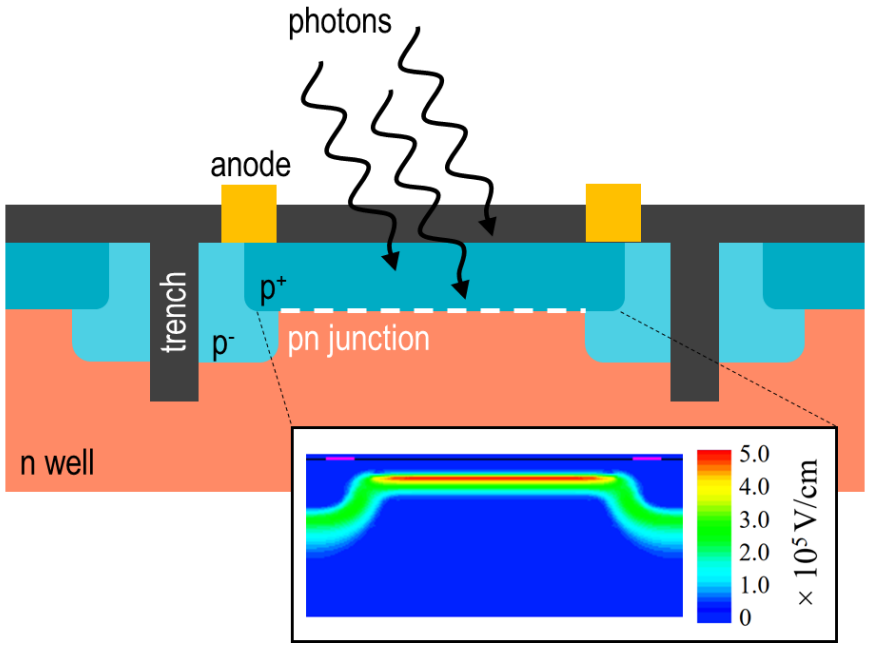

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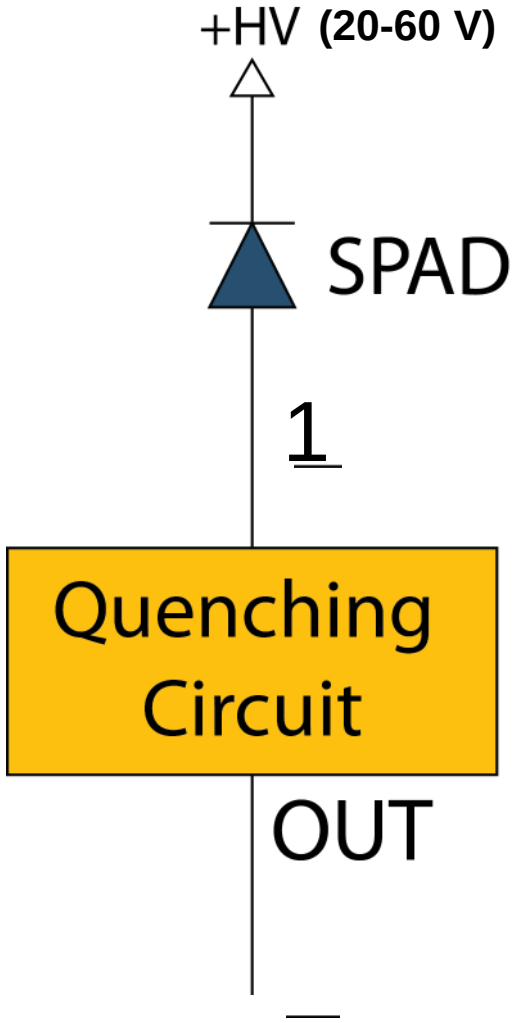

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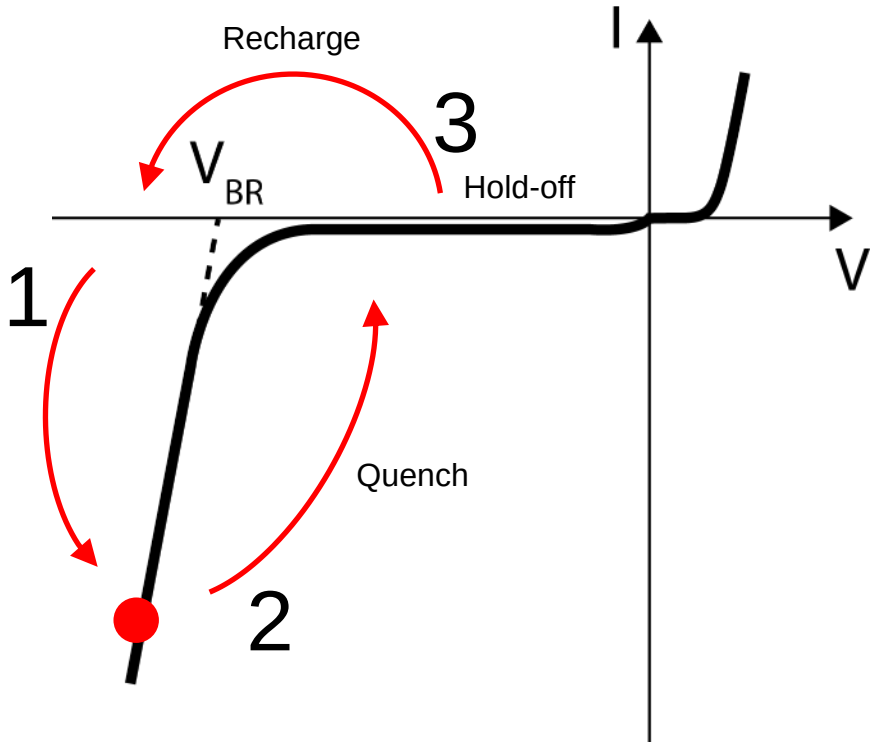

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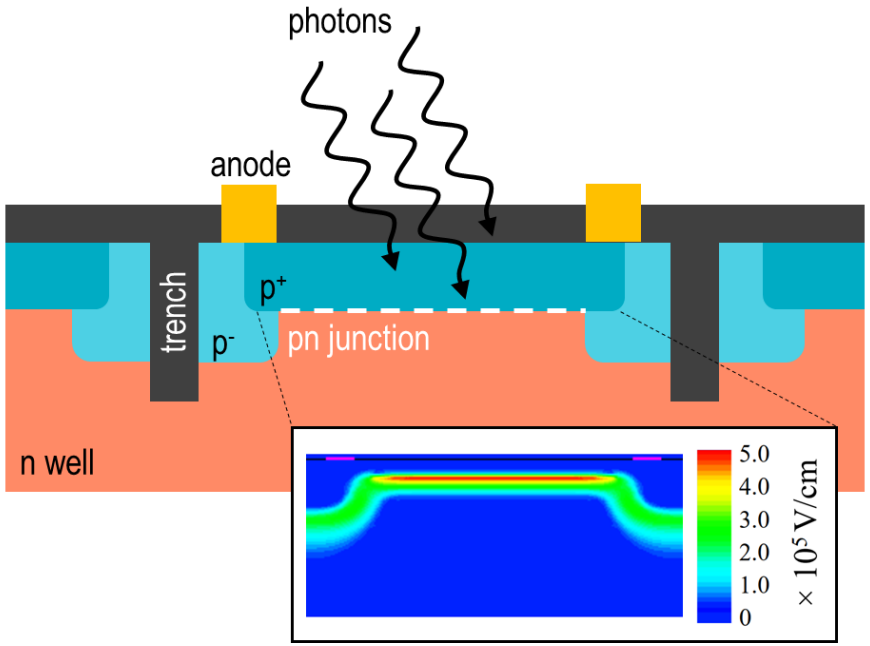

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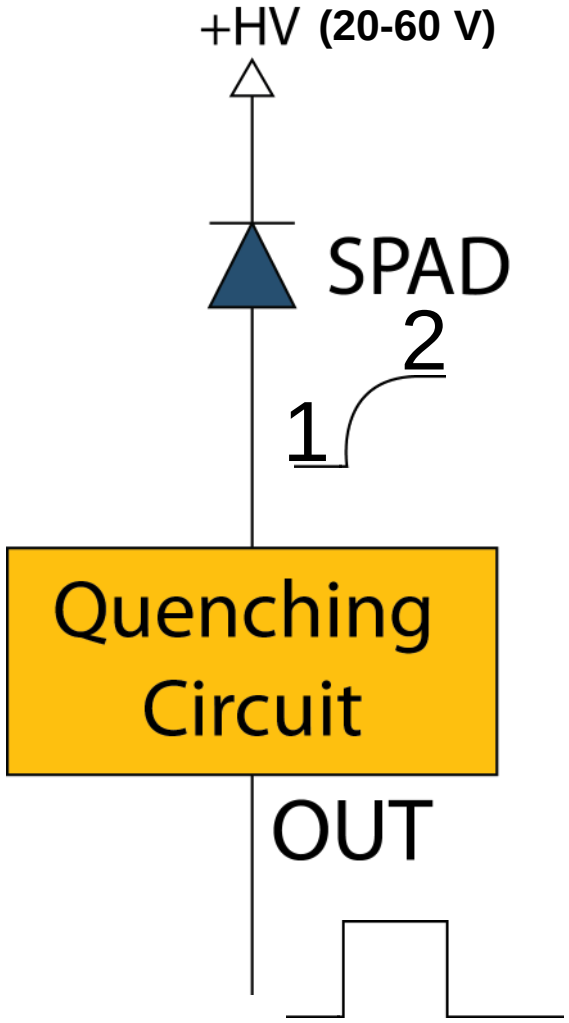

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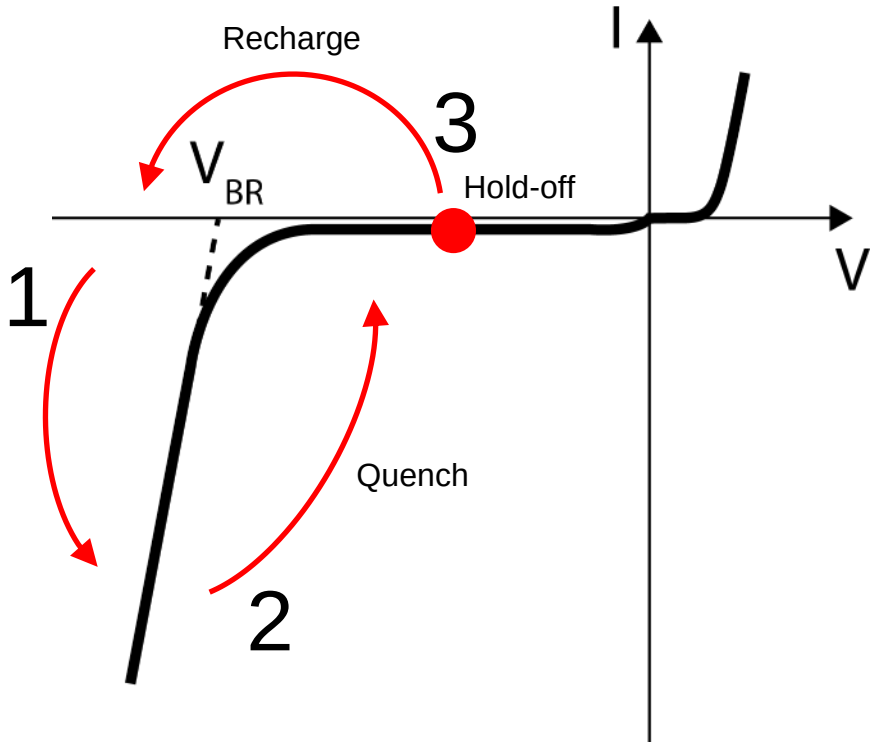

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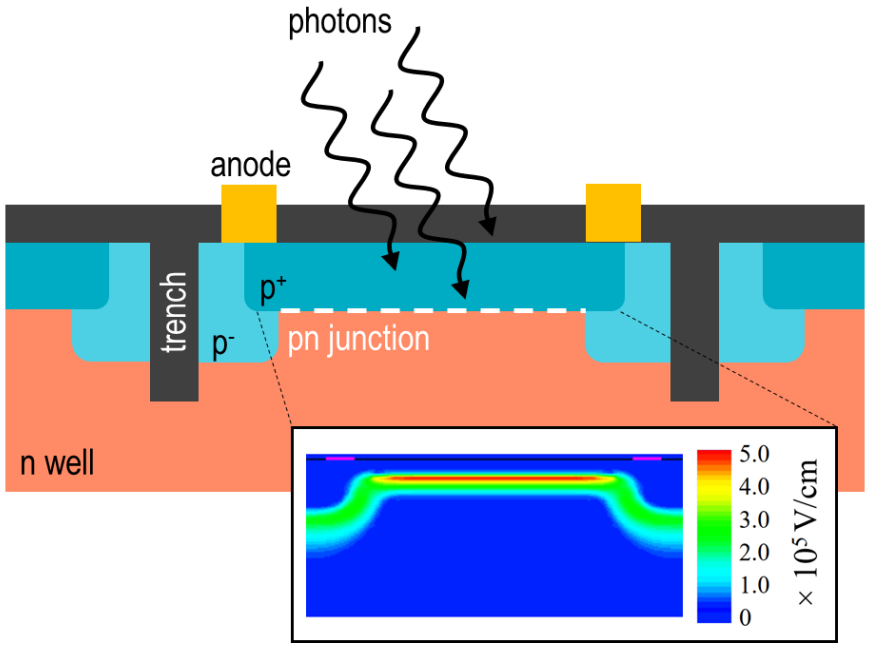

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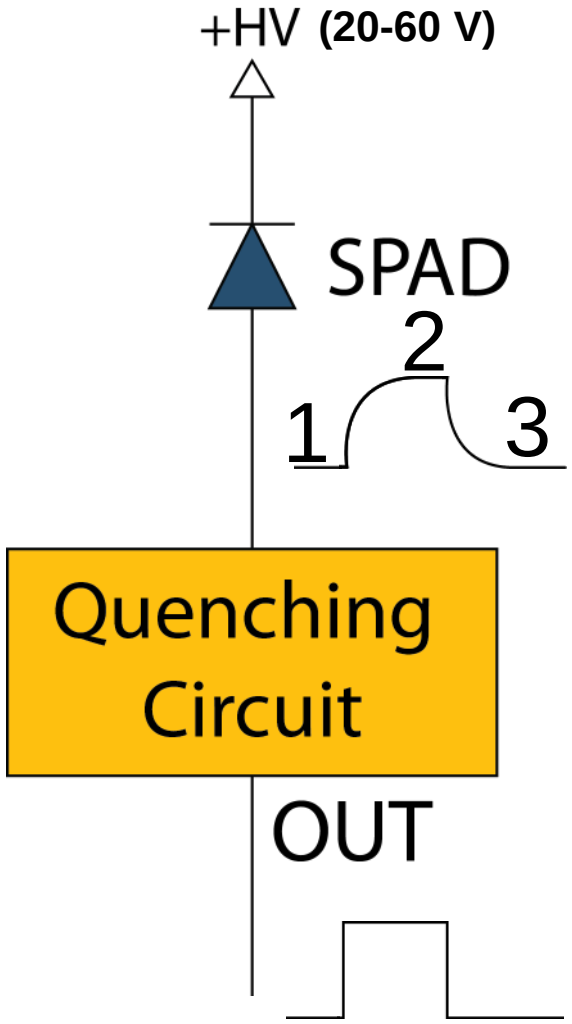

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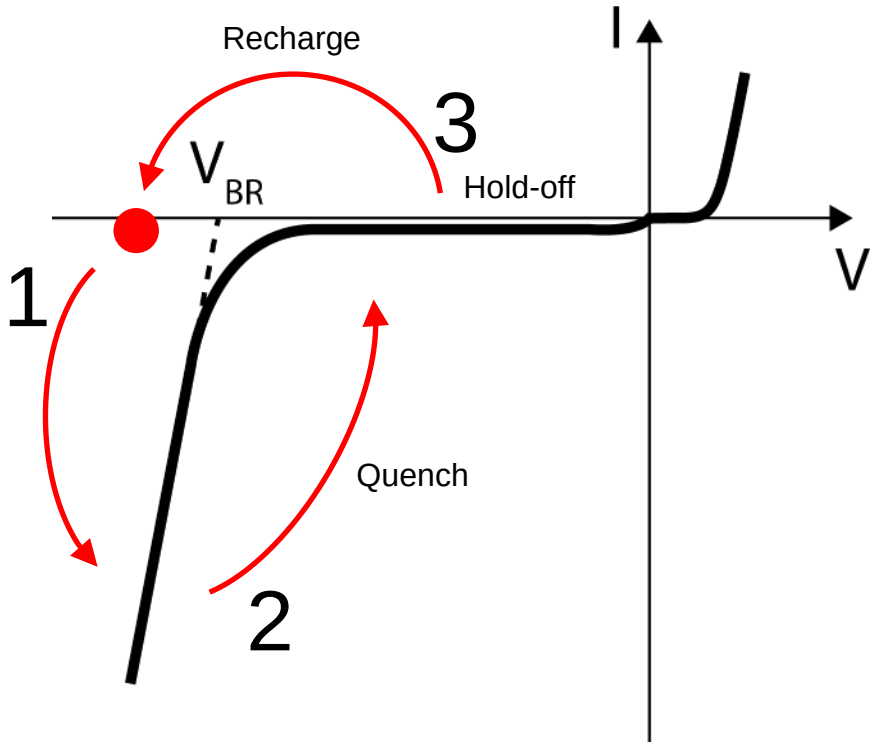

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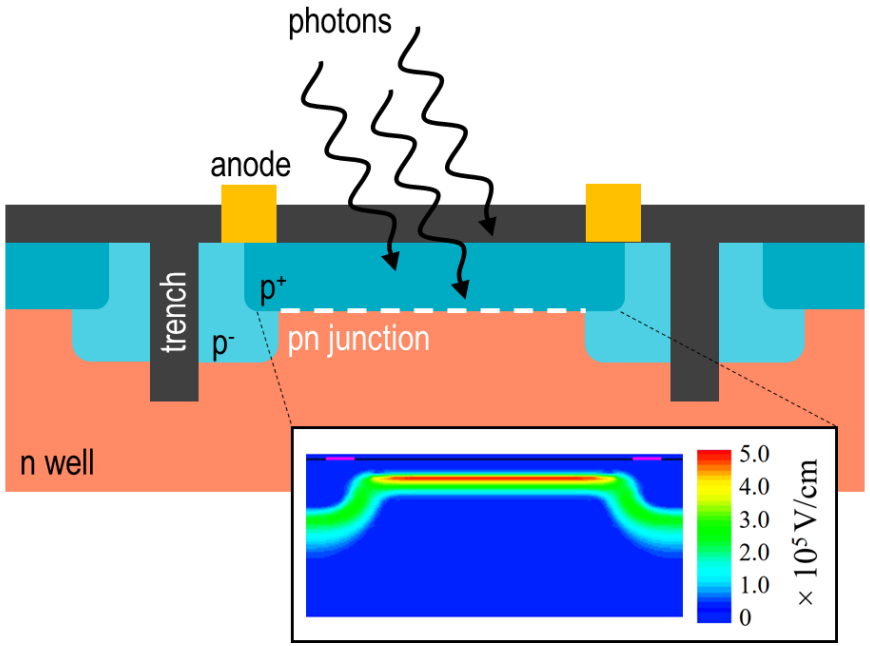

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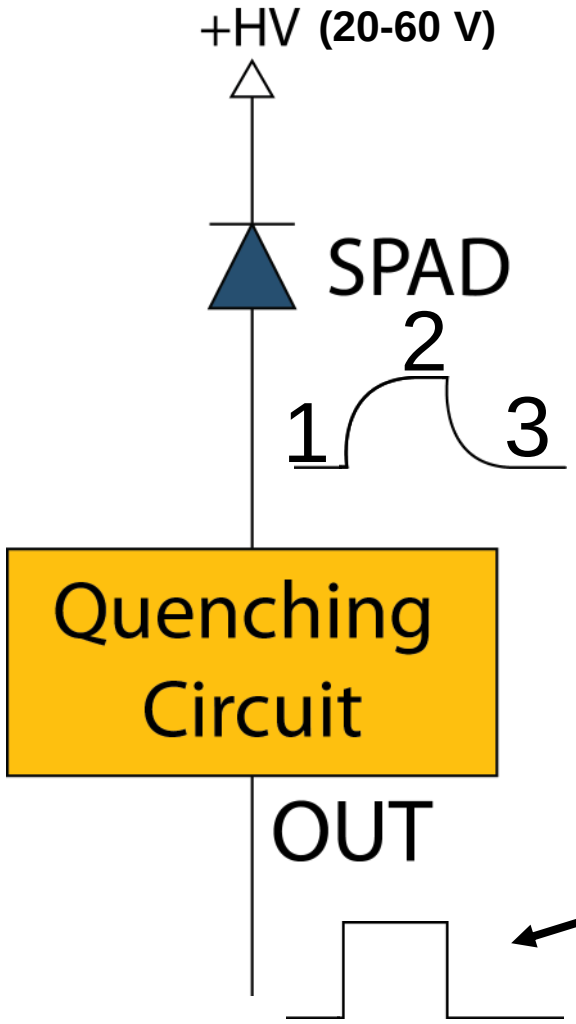

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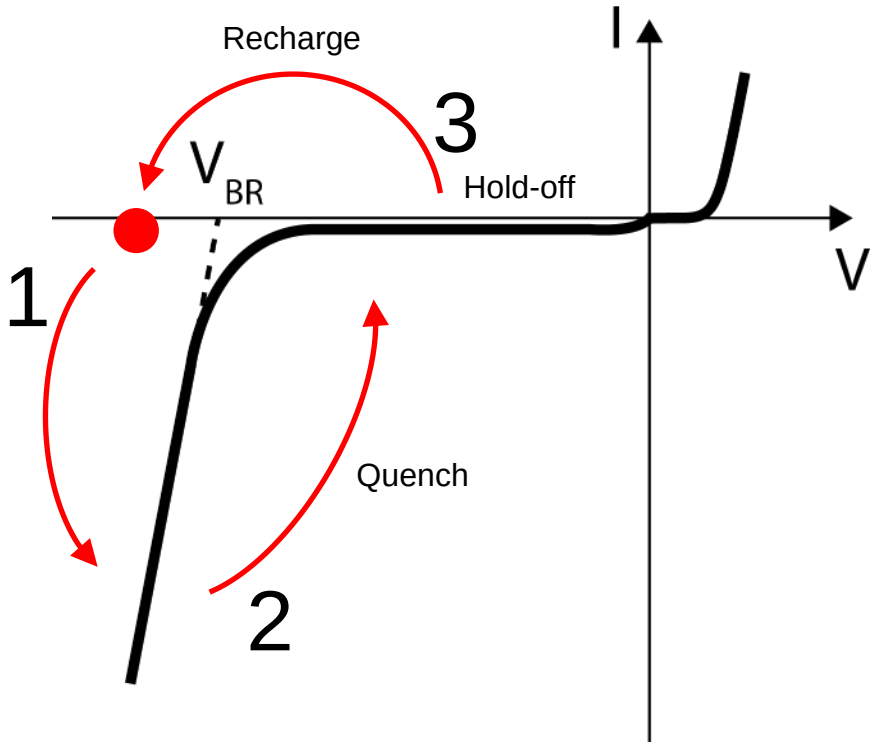

Response of the SPAD is binary

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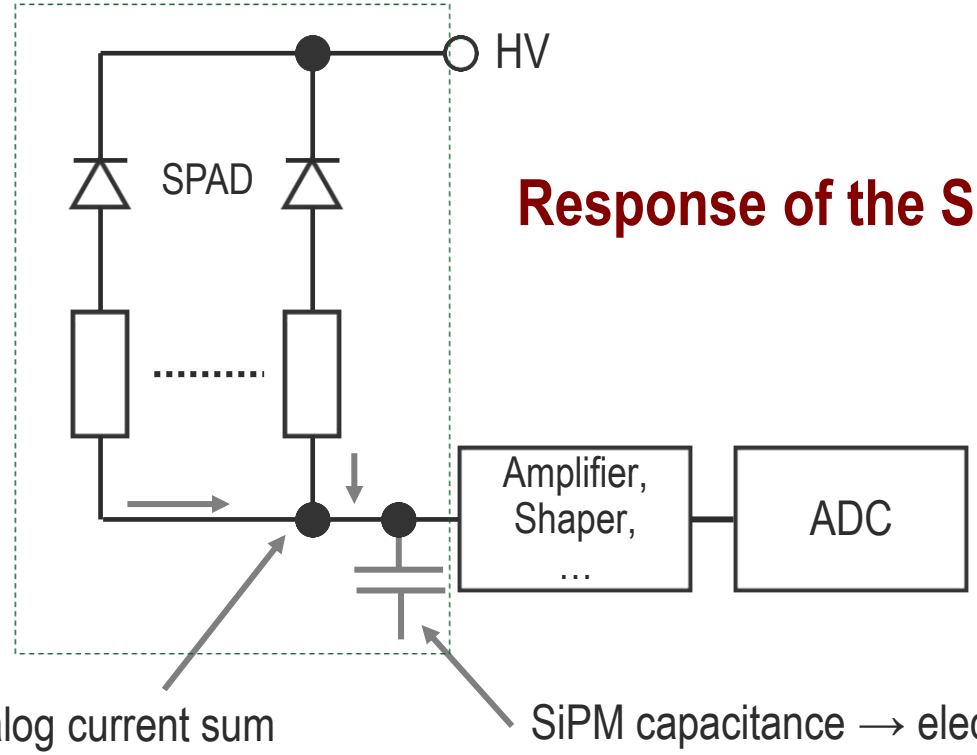
ANALOG SIPM VS DIGITAL SIPM

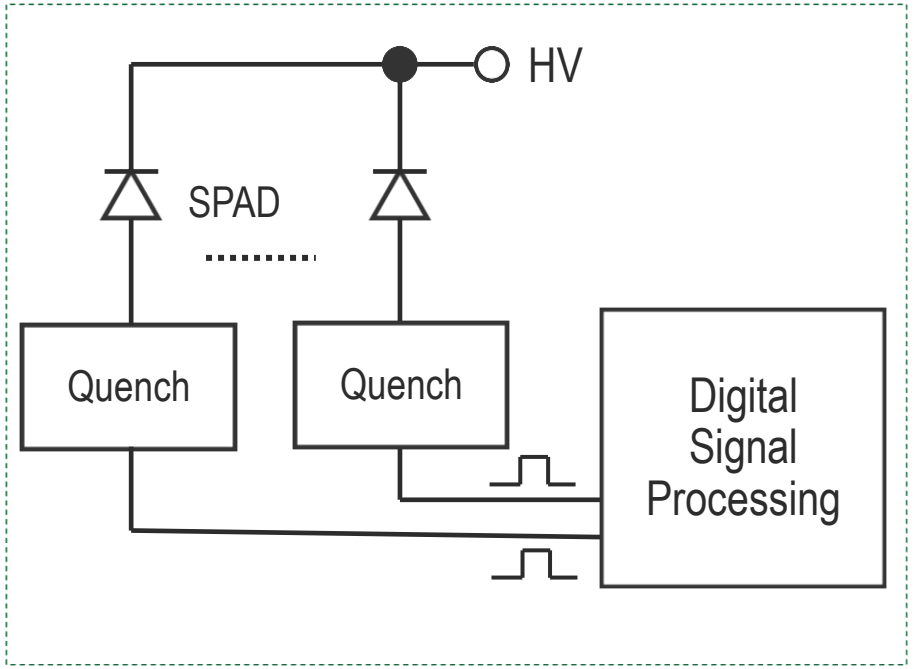
SiPM : Silicon Photo Multiplier

Analog SiPM



Response of the SPAD is binary

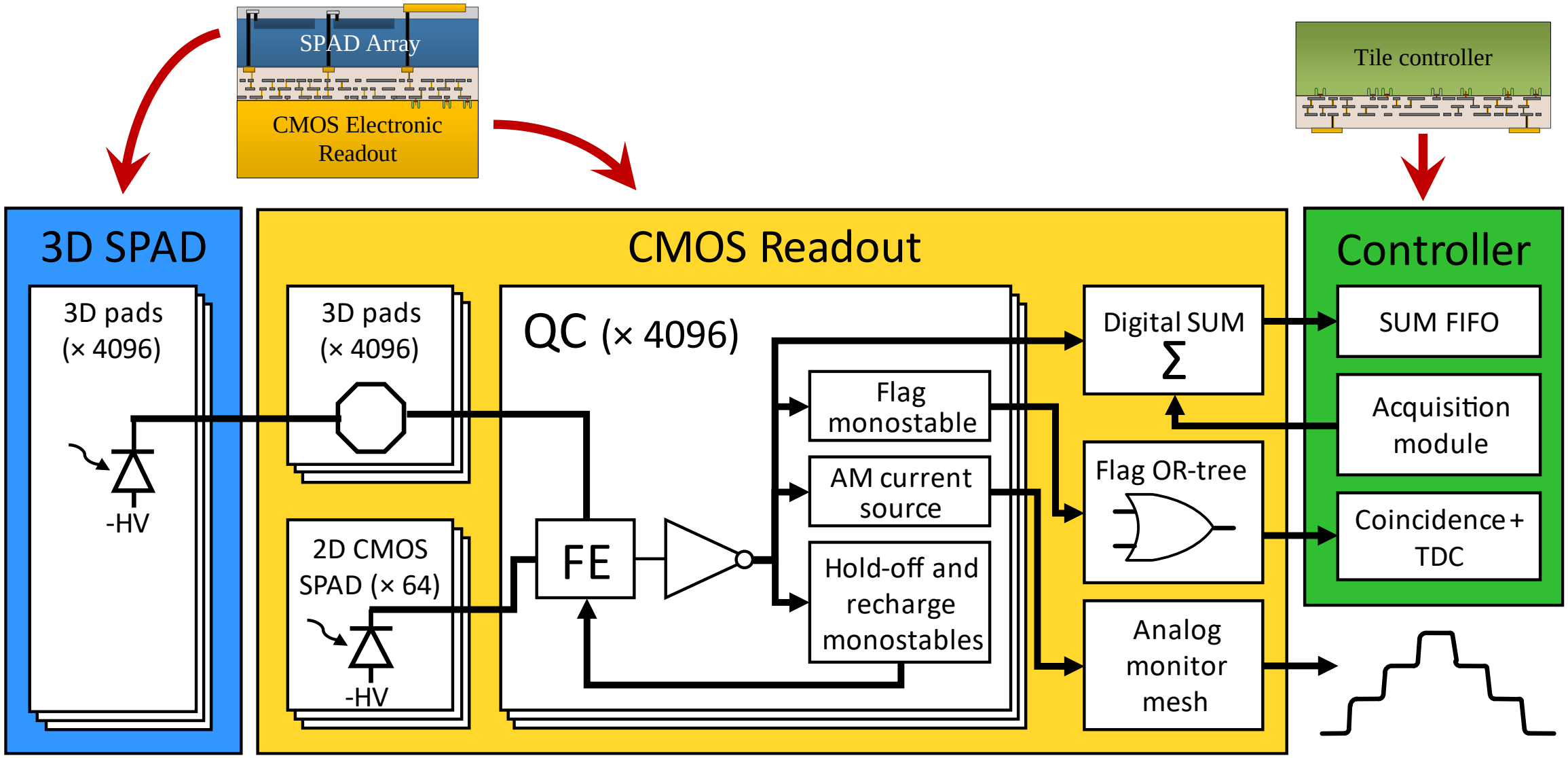
Photon to Digital Converter (aka Digital SiPM)



The amplifier transforms charge into voltage and then BACK to digital.

Individual SPAD readout, no D/A+A/D conversion. Everything stays digital.

PHOTON-TO-DIGITAL CONVERTER: ARCHITECTURE



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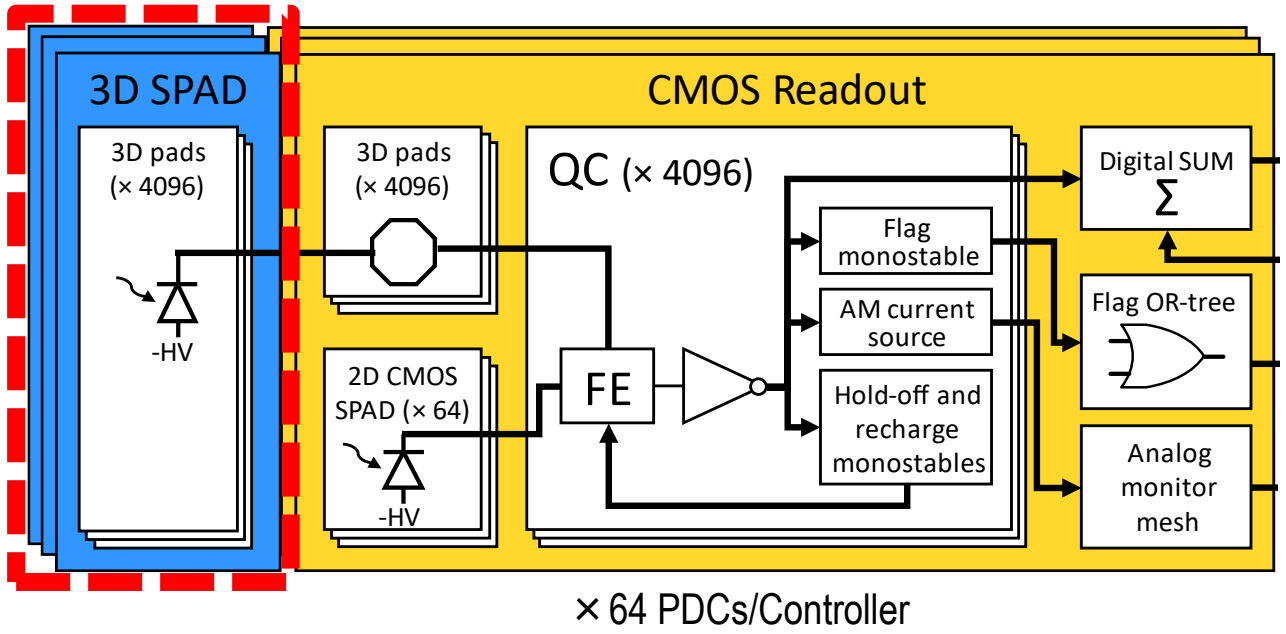
PHOTON-TO-DIGITAL CONVERTER: ARCHITECTURE

3D SPAD

- 4096 SPAD
- 3D pads
- HV at the anode



PHOTON-TO-DIGITAL CONVERTER: ARCHITECTURE

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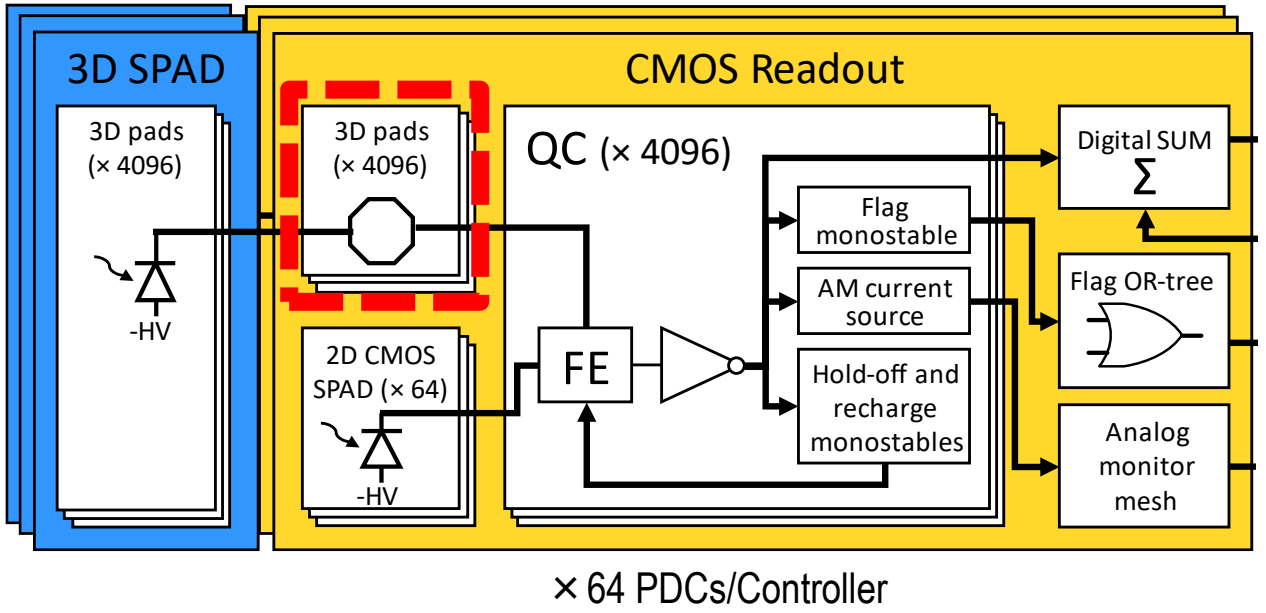
CMOS readout pads

- 3D pads (X 4096)
- Individual quenching circuit for each SPAD



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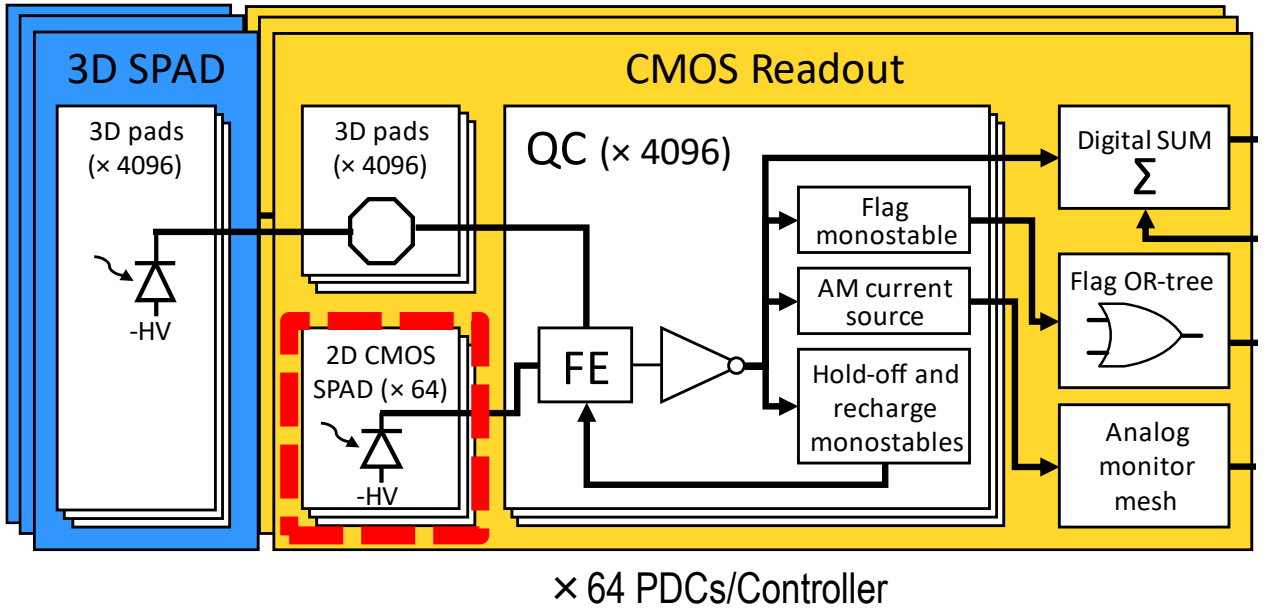
2D CMOS SPAD

- 64 SPAD on CMOS readout
- Individually quenched



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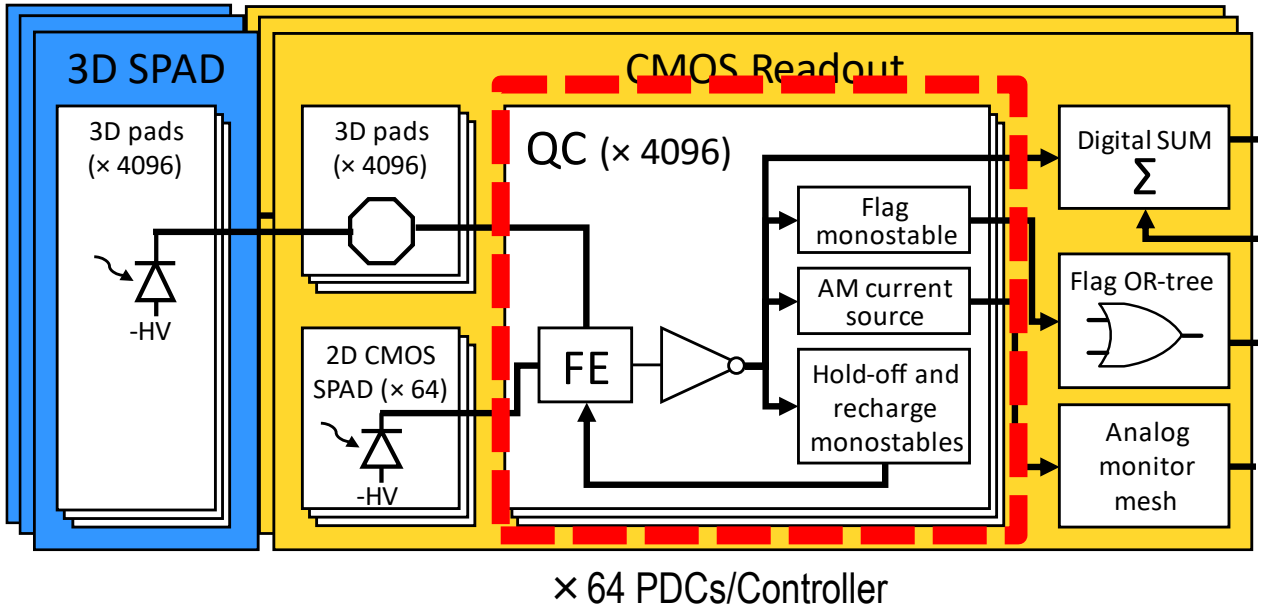
2D CMOS SPAD

- 64 SPAD on CMOS readout
- Individually quenched



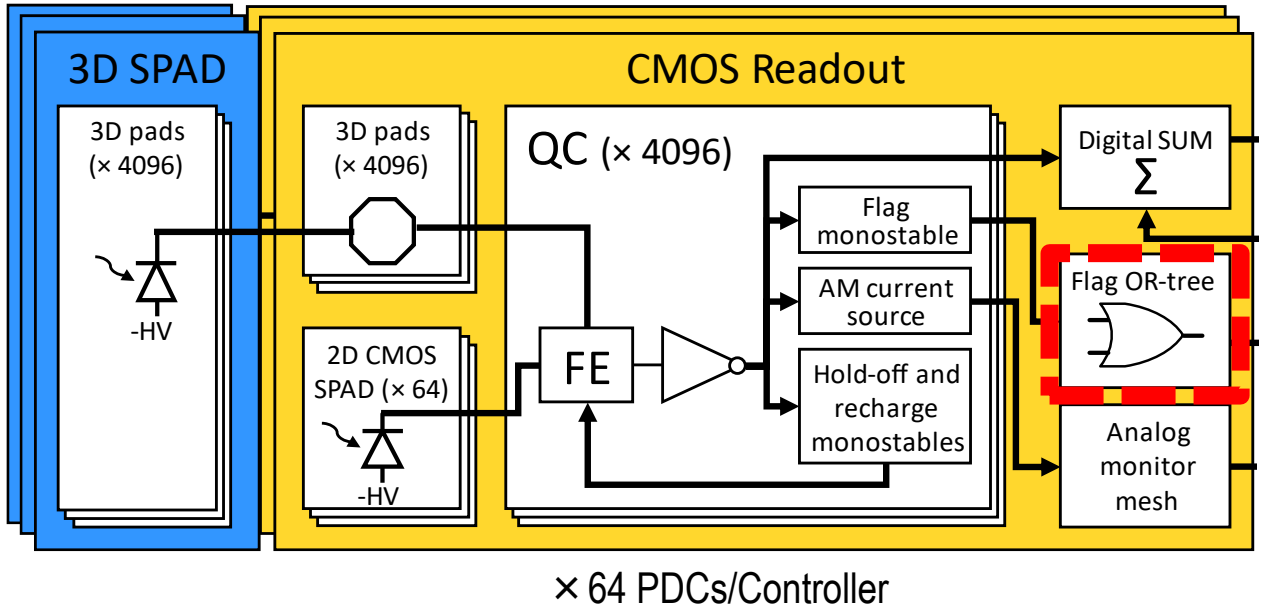
Quenching circuit

- Read the SPAD from the cathode
- Send the flag
- Hold-off et recharge the SPAD

PHOTON-TO-DIGITAL CONVERTER: ARCHITECTURE

Flag output

- Pulsed output (adjustable from few ns to tens of ns).
- From an OR-tree.
- Timing jitter better than 100 ps RMS.



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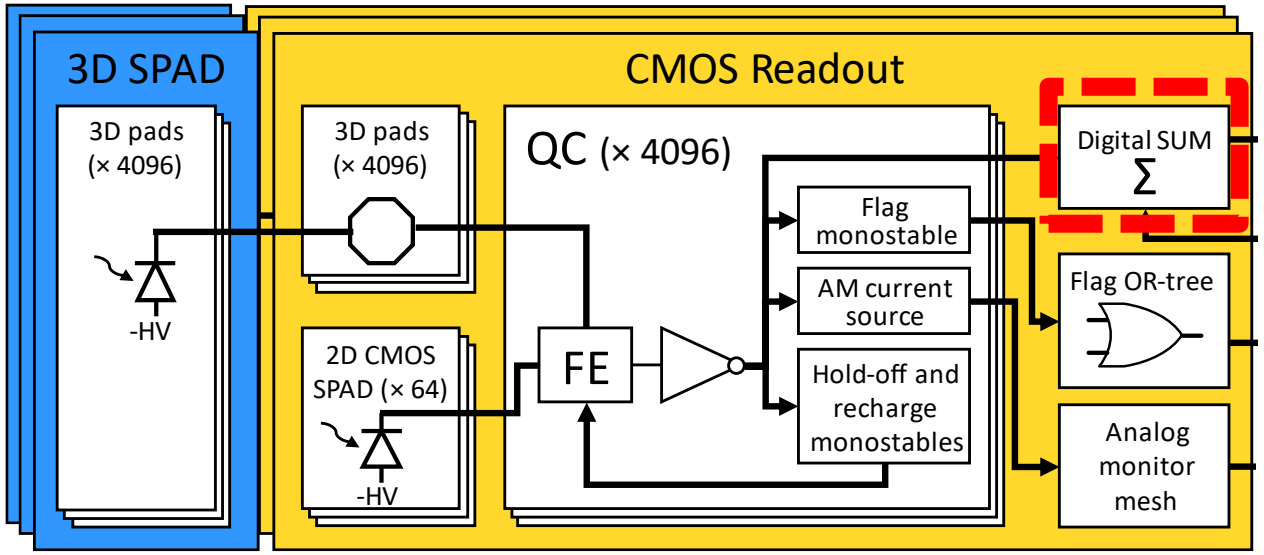
Digital Sum

- Digital count of triggered SPADs inside a bin (dynamic range of 4096 photons).
- Adjustable bin width from 10 ns up to µs.
- Internal FIFO of 128 bins.



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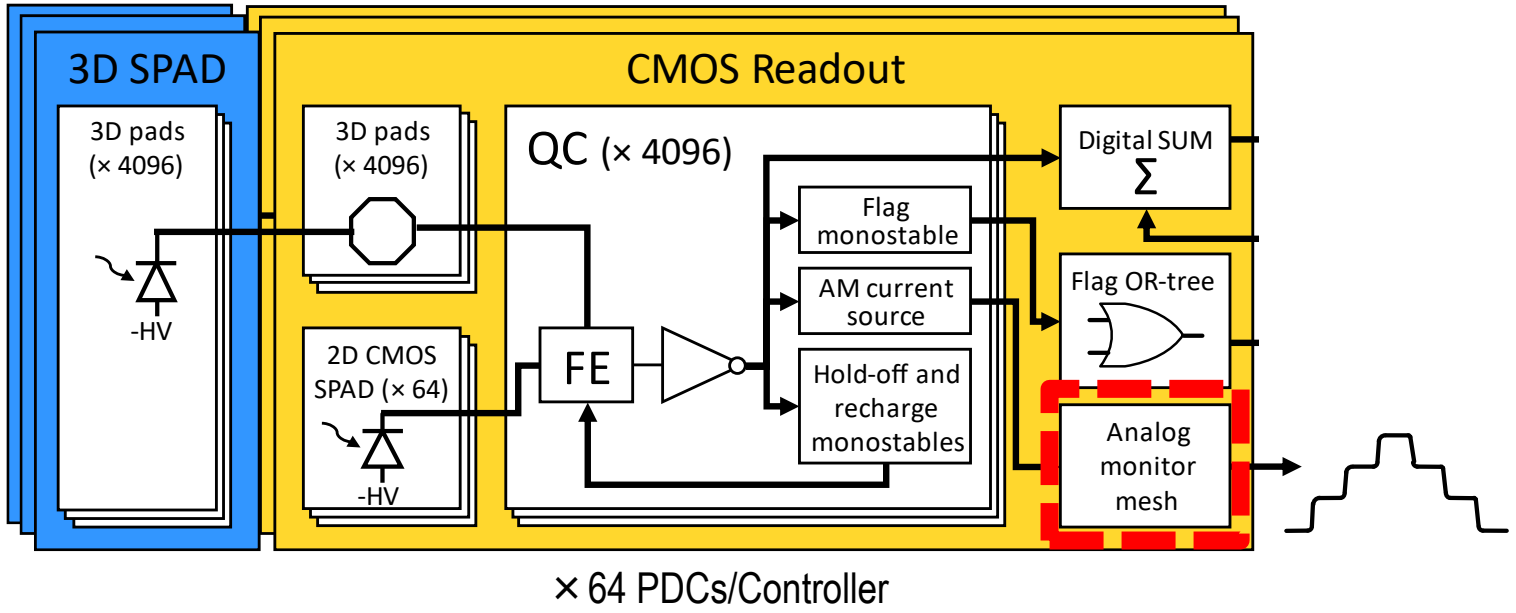
Analog Monitor

- Current proportional to triggered SPADs.



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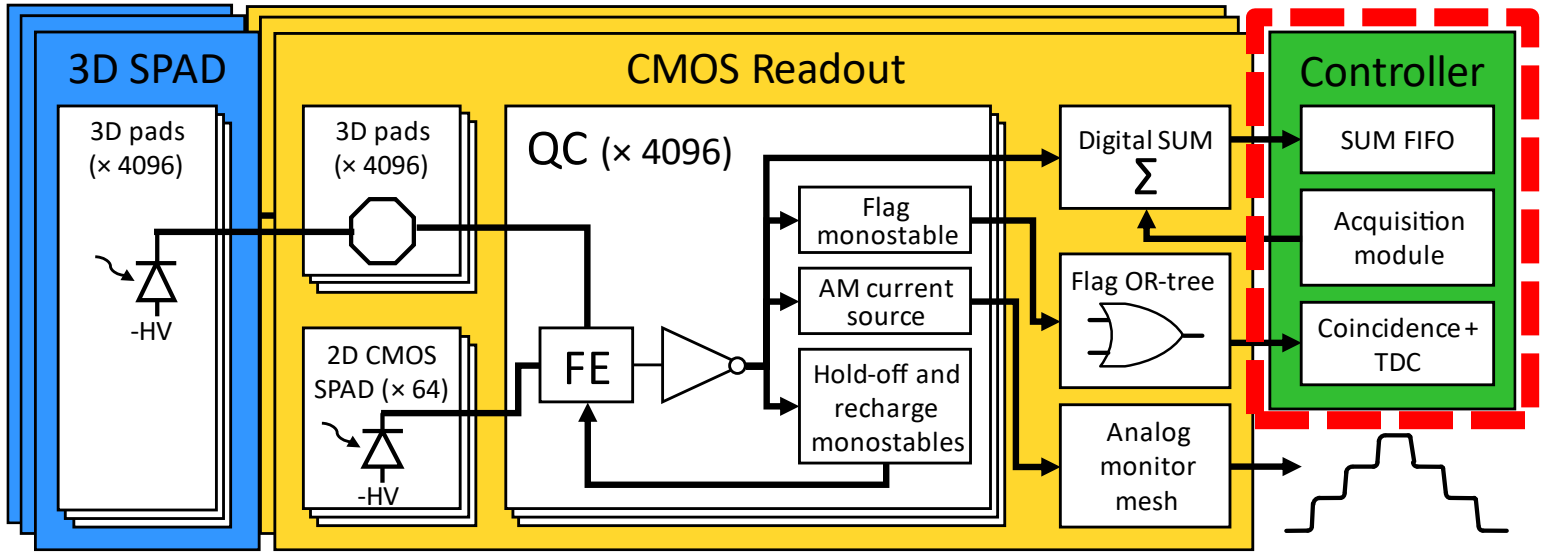
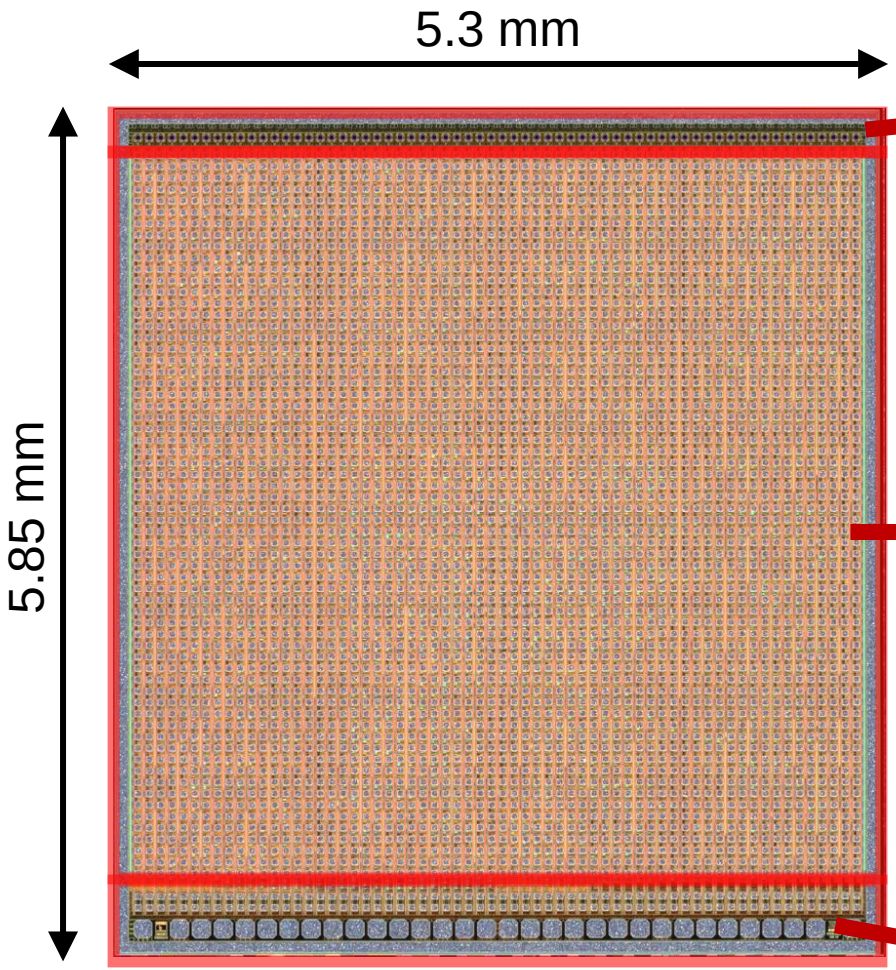


Controller (1 for 64 PDCs)

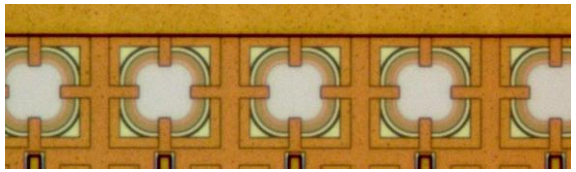
- Start PDC acquisition, based on the number of flag received to discriminate dark count.
- Bank of TDCs for timing measurements on flags.
- Receives data from PDCs and includes post-processing.
- Communicate with an external computer.

PDC: FABRICATED CMOS READOUT

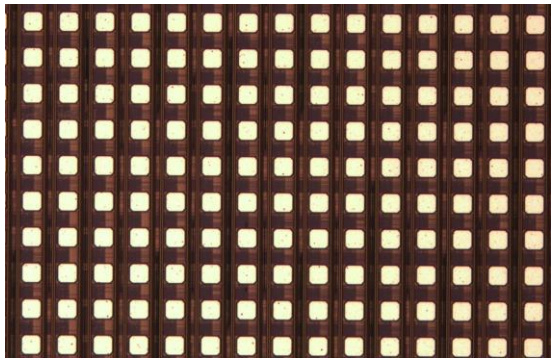


PDC CMOS READOUT

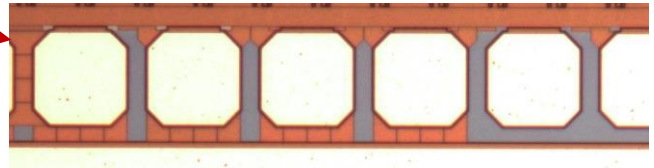
64x 2D CMOS SPADs



64 × 64 quench circuits ready for 3D integration



IO pads ESD protected



Key Specifications

- TSMC 180 nm BCD CMOS process.
- 78 µm SPAD-to-SPAD pitch for a 5X5 mm active area
- Every SPAD is controlled individually.
  - Noisy/defective SPADs can be disabled.
- Dynamic range of 0 to 4096 photons.

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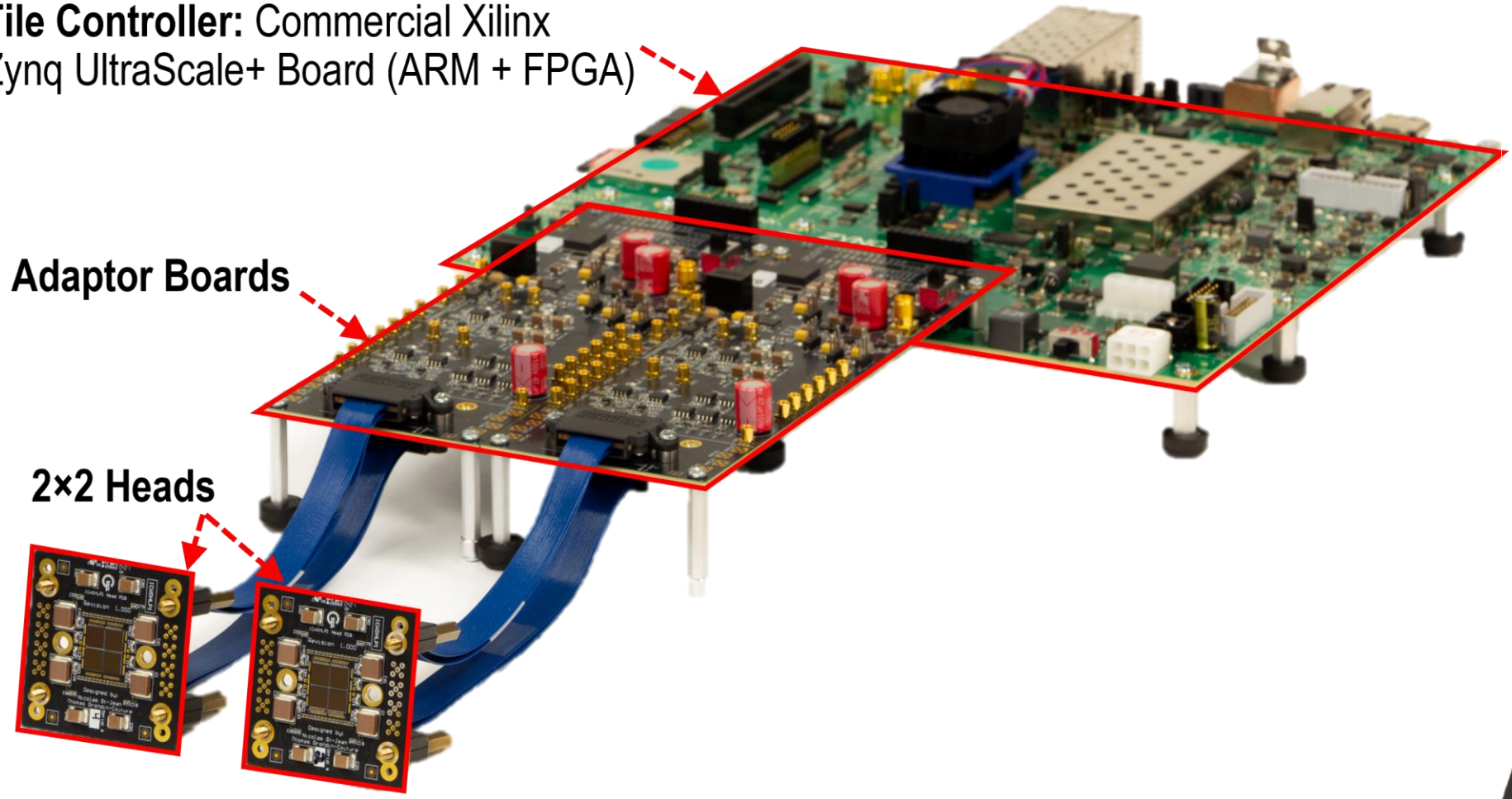
2 × 2 PHOTODETECTION MODULE

Tile Controller: Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

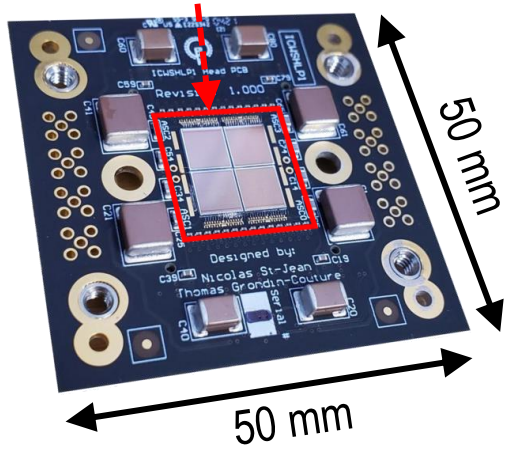
Adaptor Boards

2×2 Heads

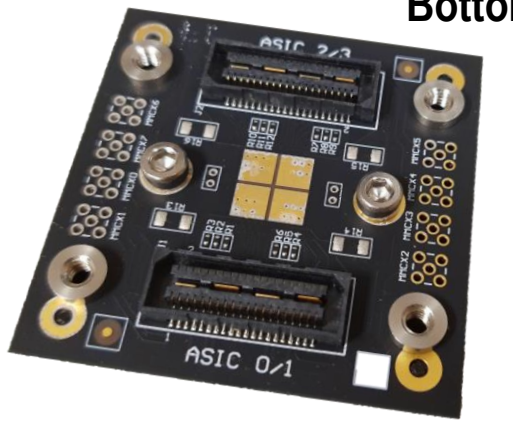


2 × 2 PDCs

Top



Bottom



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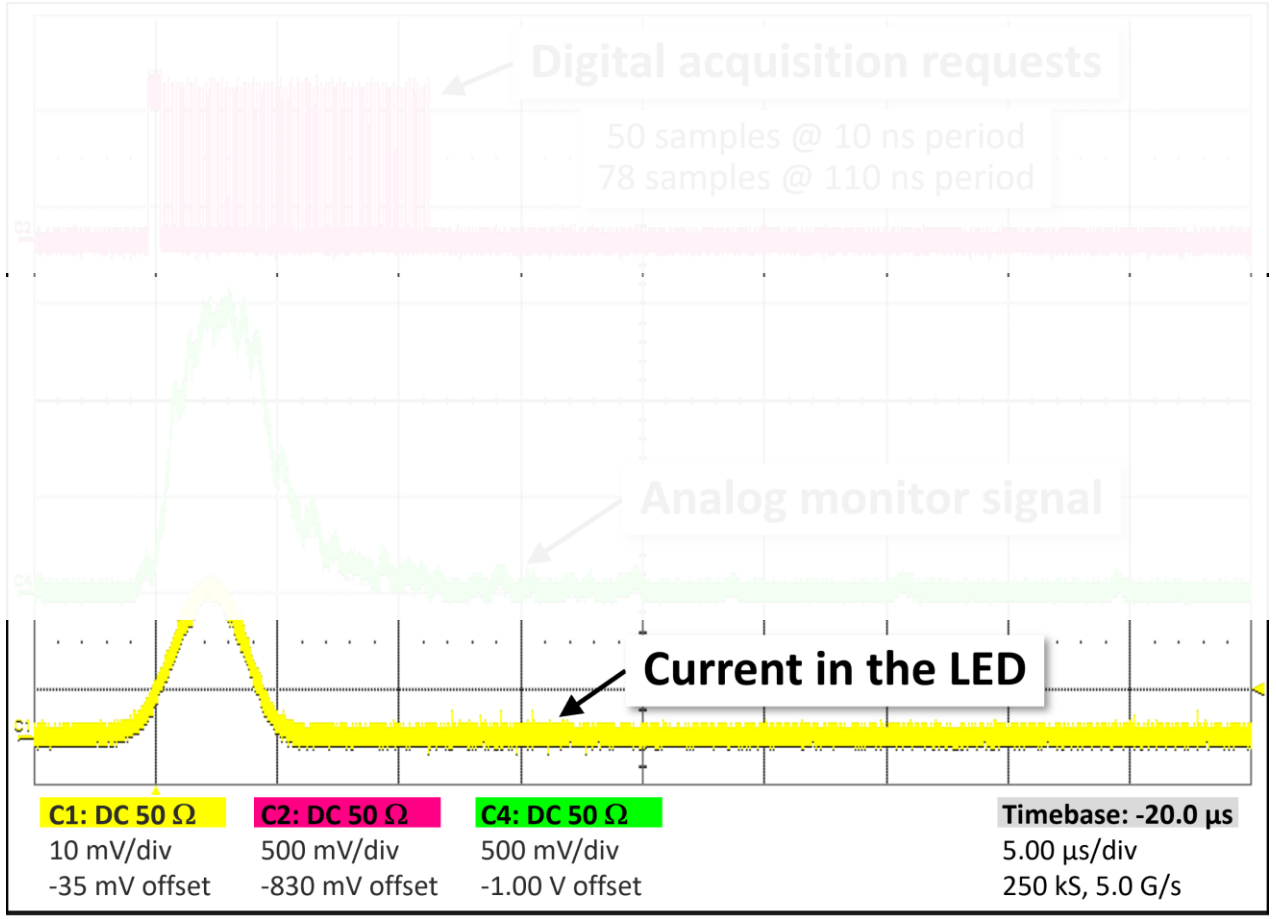
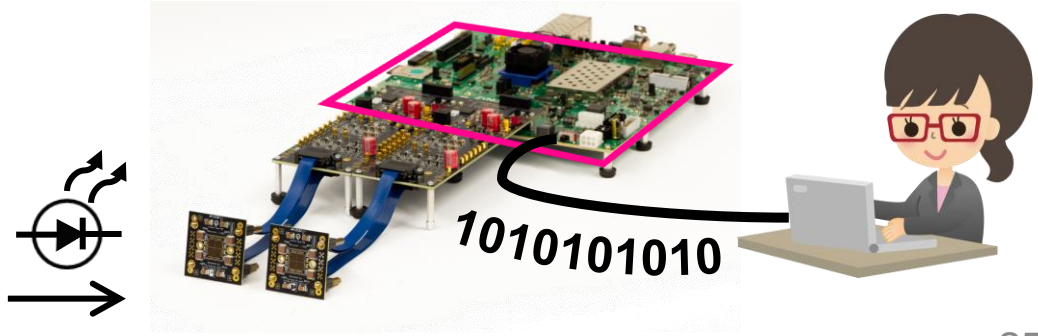
2 × 2 PHOTODETECTION MODULE WITH LED TESTING



Using embedded CMOS test SPADs of the PDC

Current in the LED to trigger the SPADs

- Driven by a waveform generator



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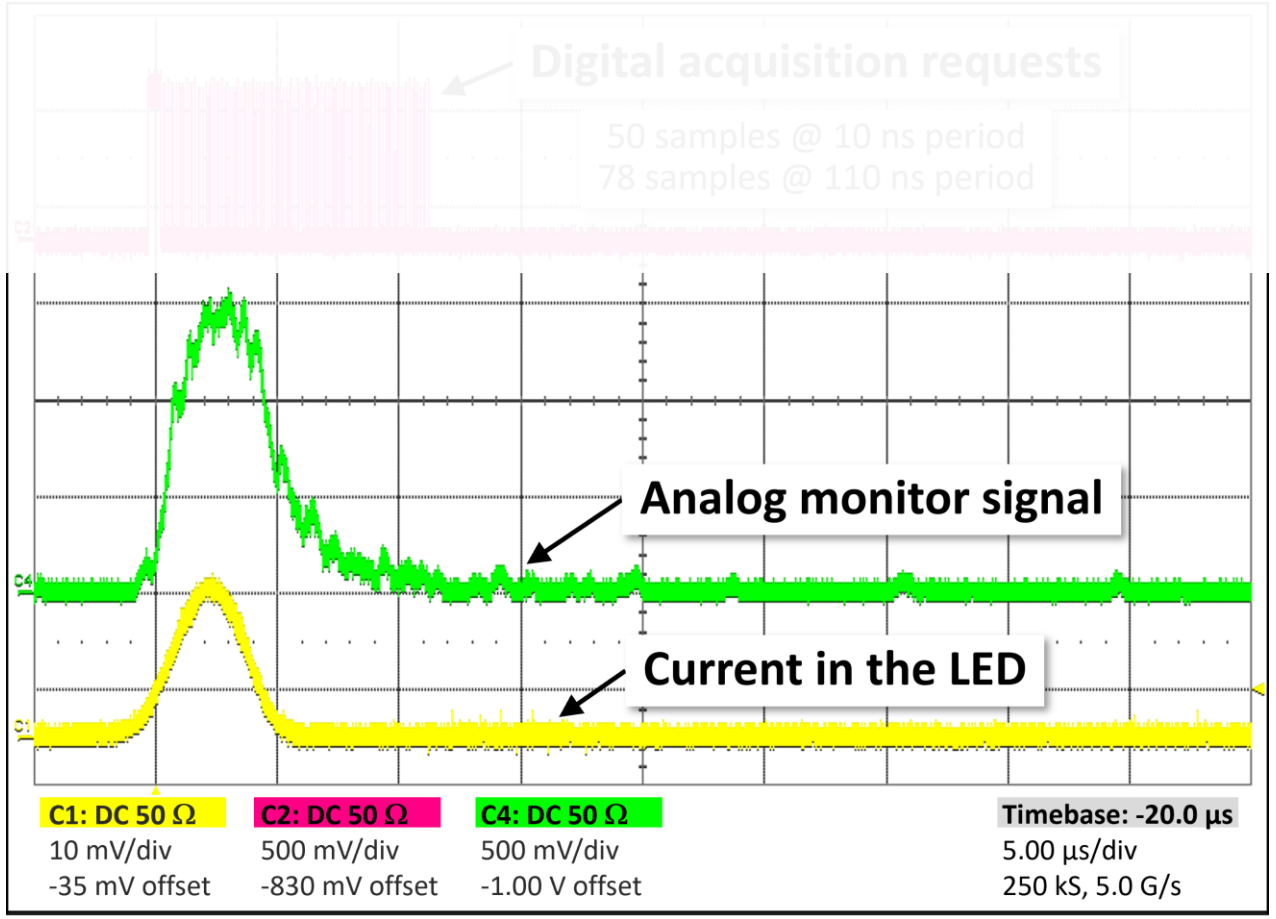

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Current in the LED to trigger the SPADs

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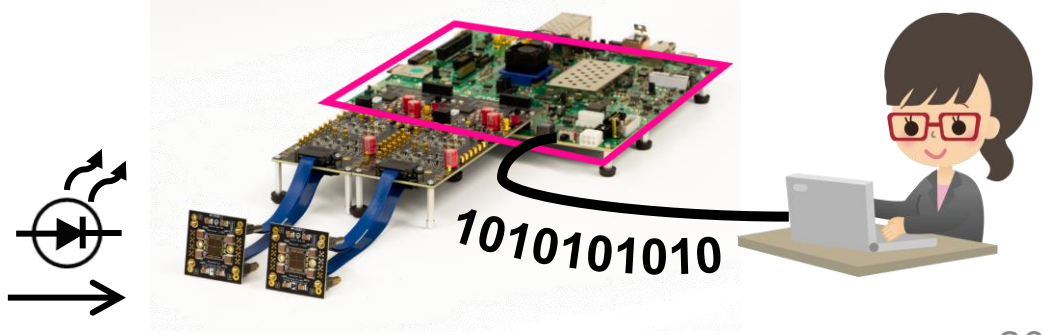
Analog Monitor

- Amplitude proportional to the number of SPADs triggered



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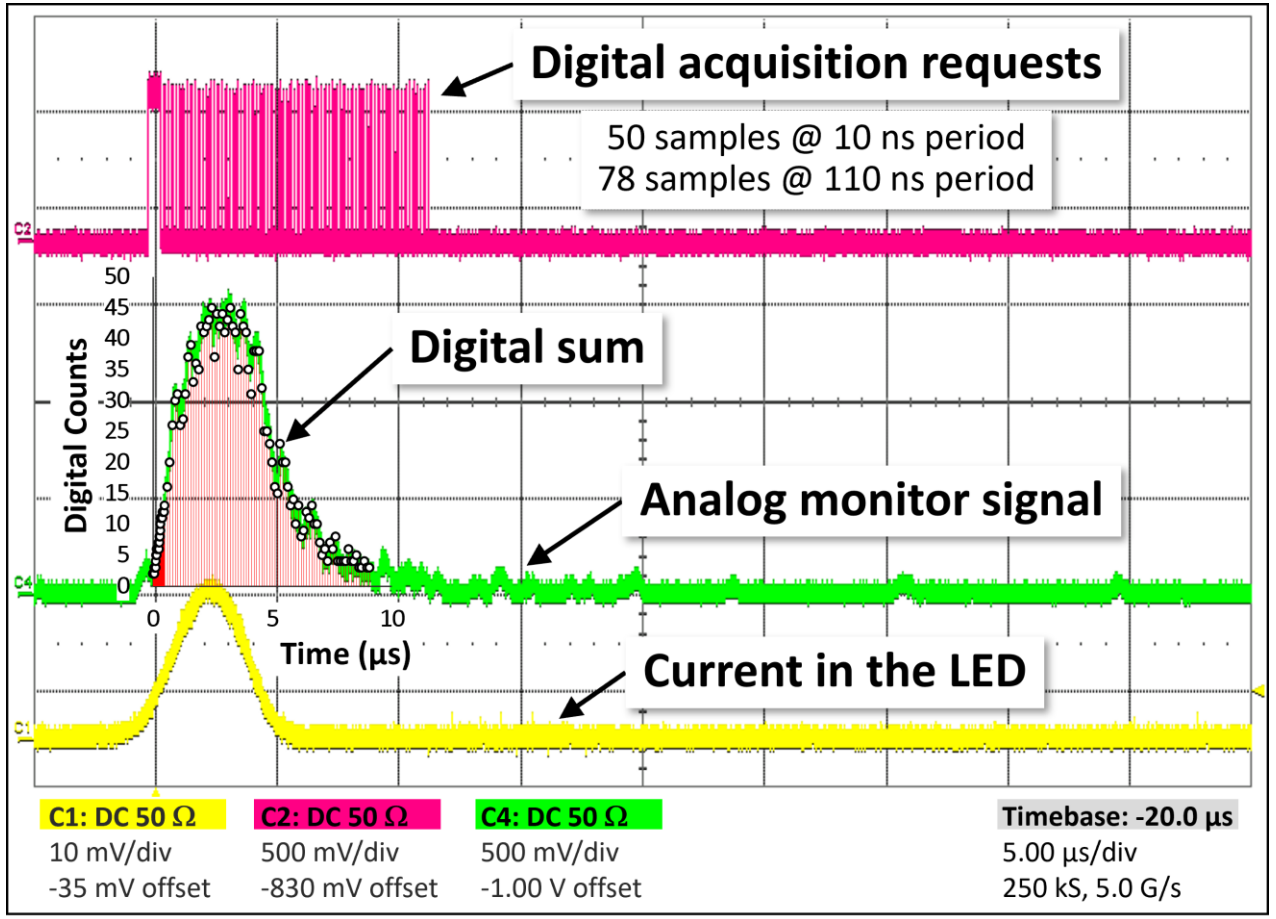
2 × 2 PHOTODETECTION MODULE WITH LED TESTING



Using embedded CMOS test SPADs of the PDC

Current in the LED to trigger the SPADs

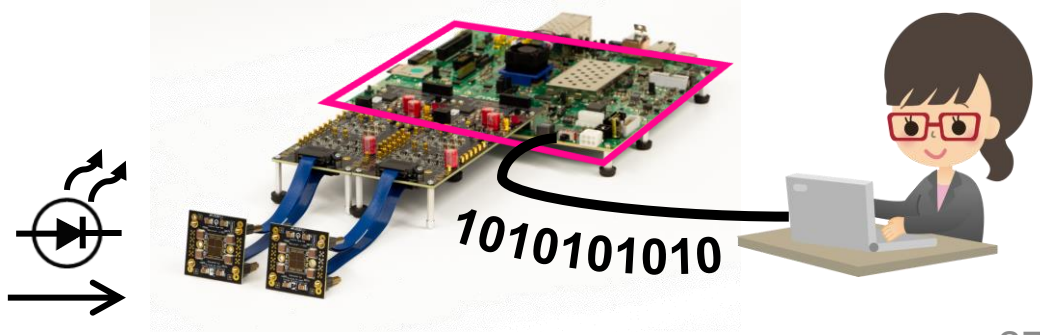
- Driven by a waveform generator

Analog Monitor

- Amplitude proportional to the number of SPADs triggered

Digital Sum Acquisition

- Based on a 100 MHz readout clock
- Generated by the FPGA (Tile Controller)



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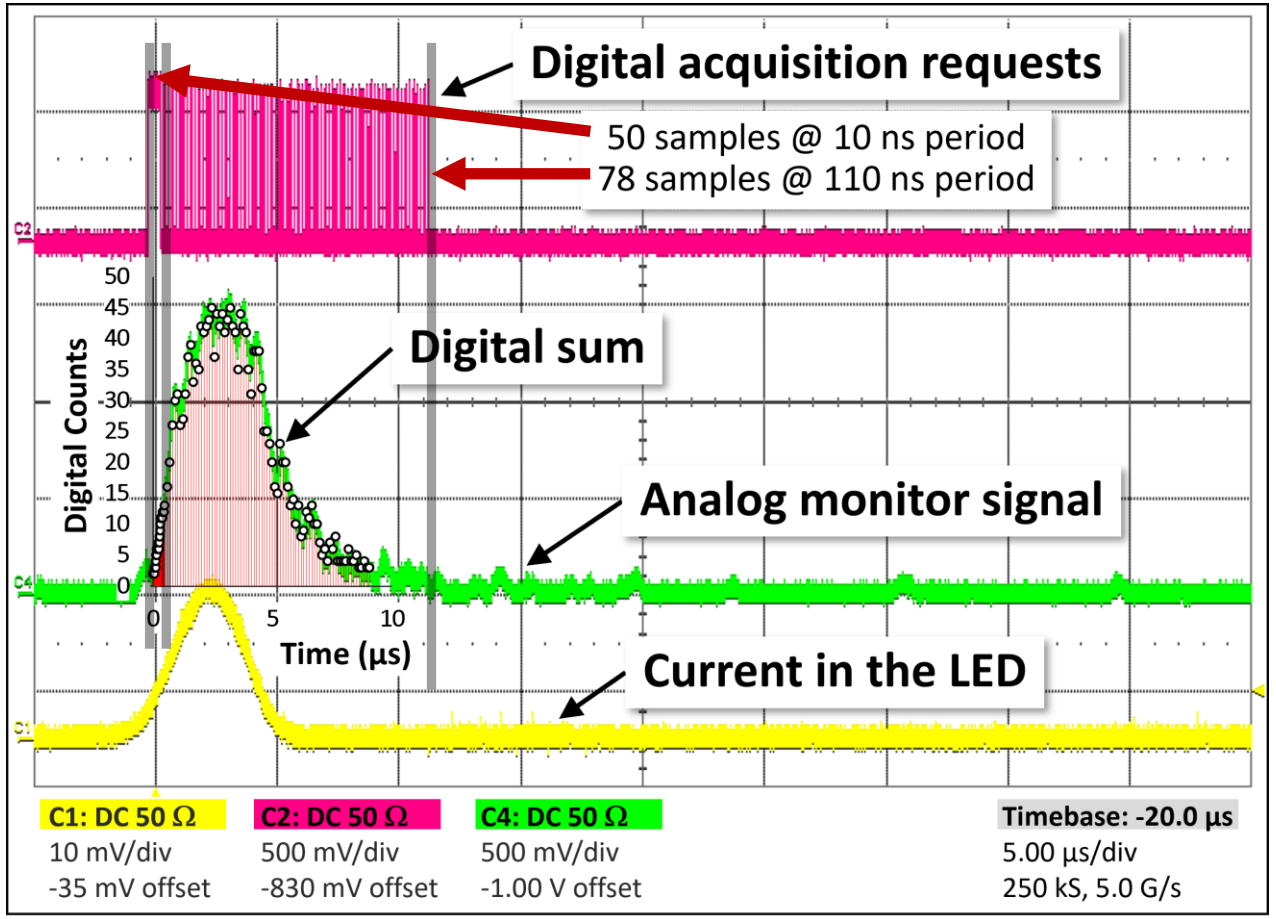

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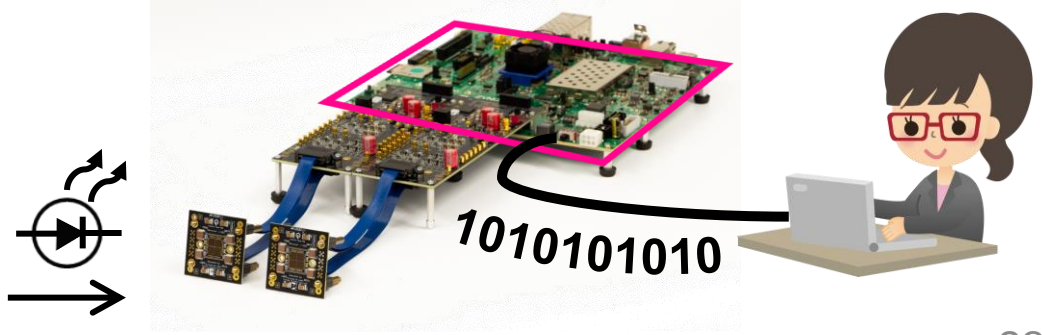

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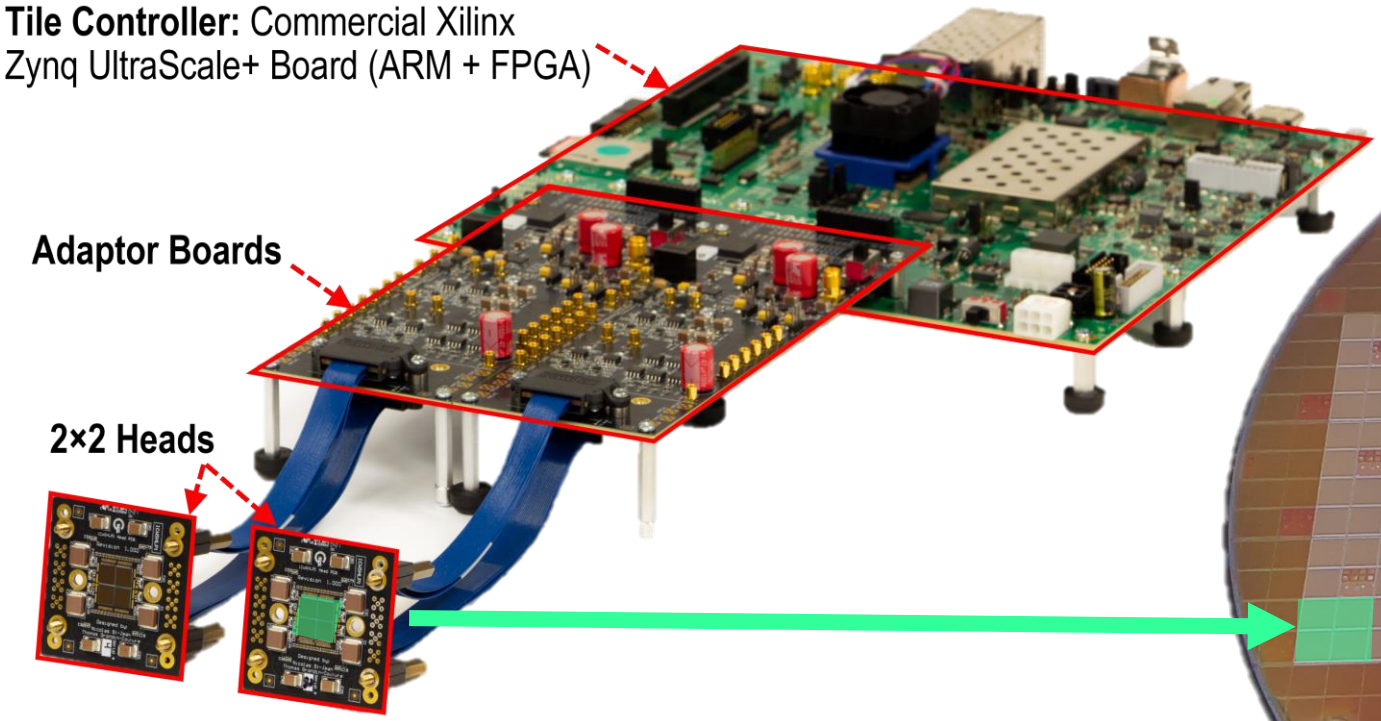
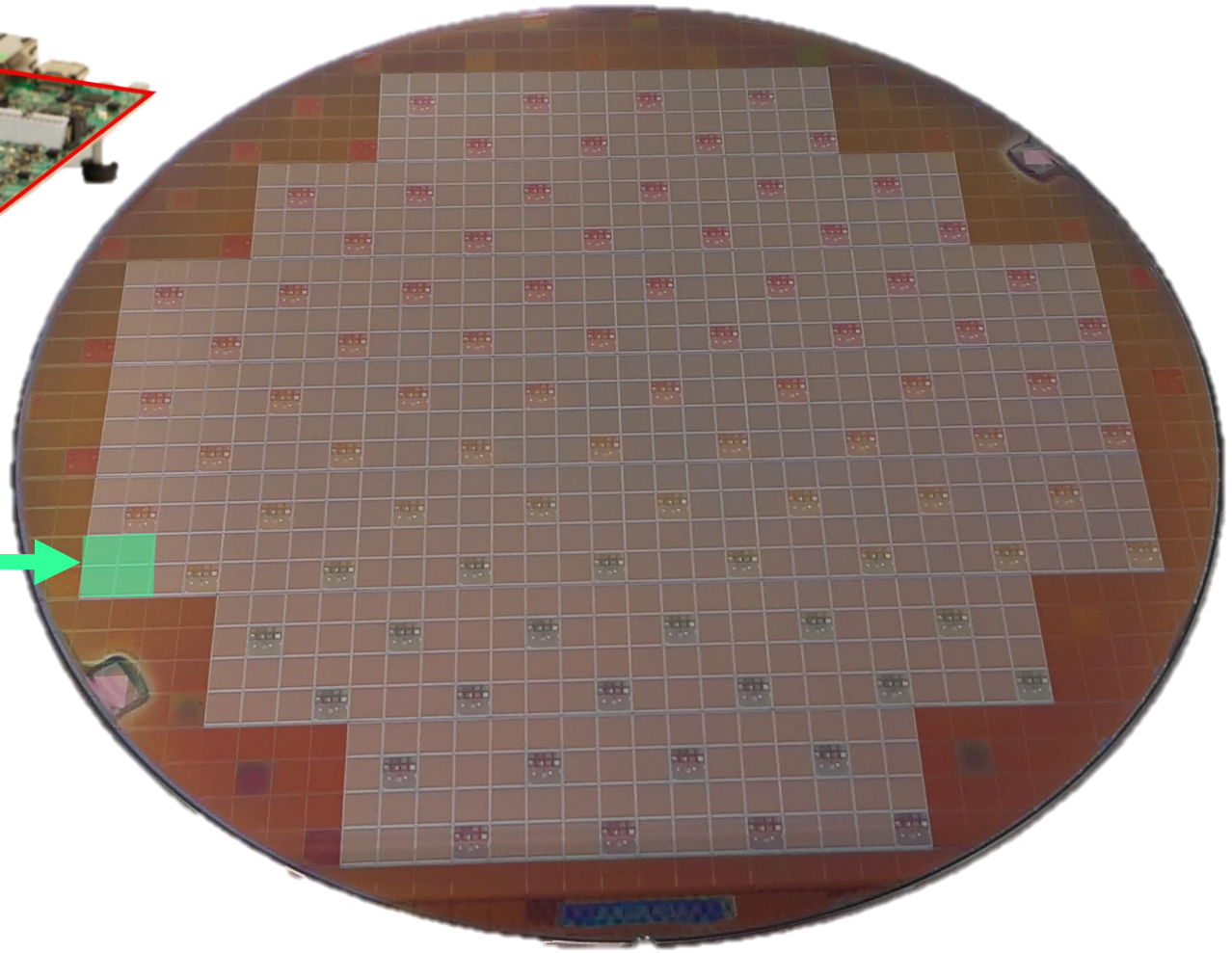
WAFER RUN OF THE PDC





200 mm wafer of PDCs

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TEST BENCH FOR WAFER-LEVEL MEASUREMENT

Probe station with probe card attach to it

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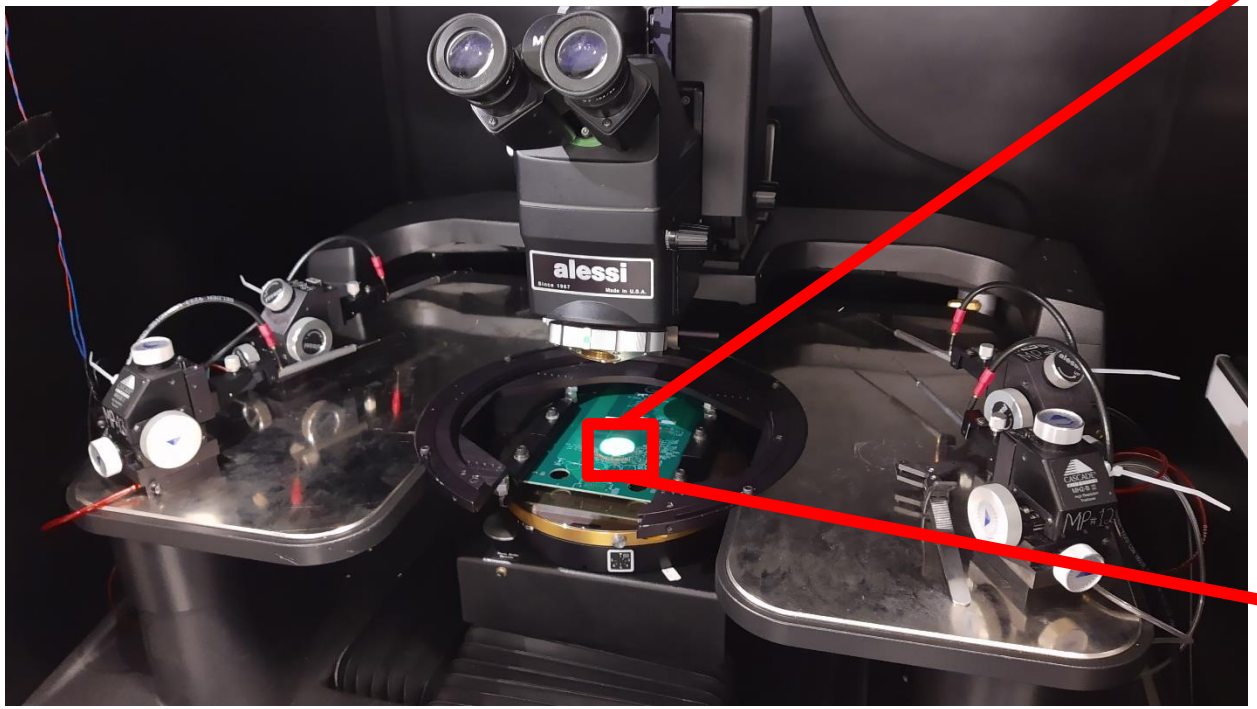
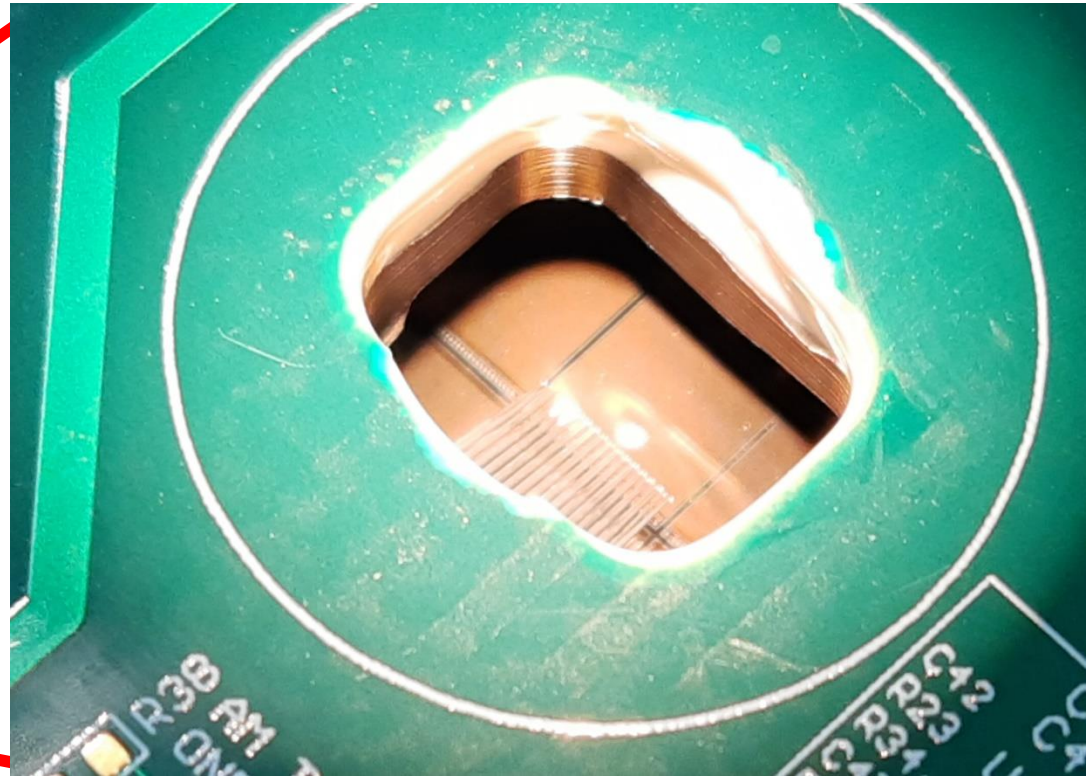
TEST BENCH FOR WAFER-LEVEL MEASUREMENT

Dedicated probe card

- Active probe card with FPGA
- Passive probe card



Probe station with probe card attach to it



Needles of the probe card

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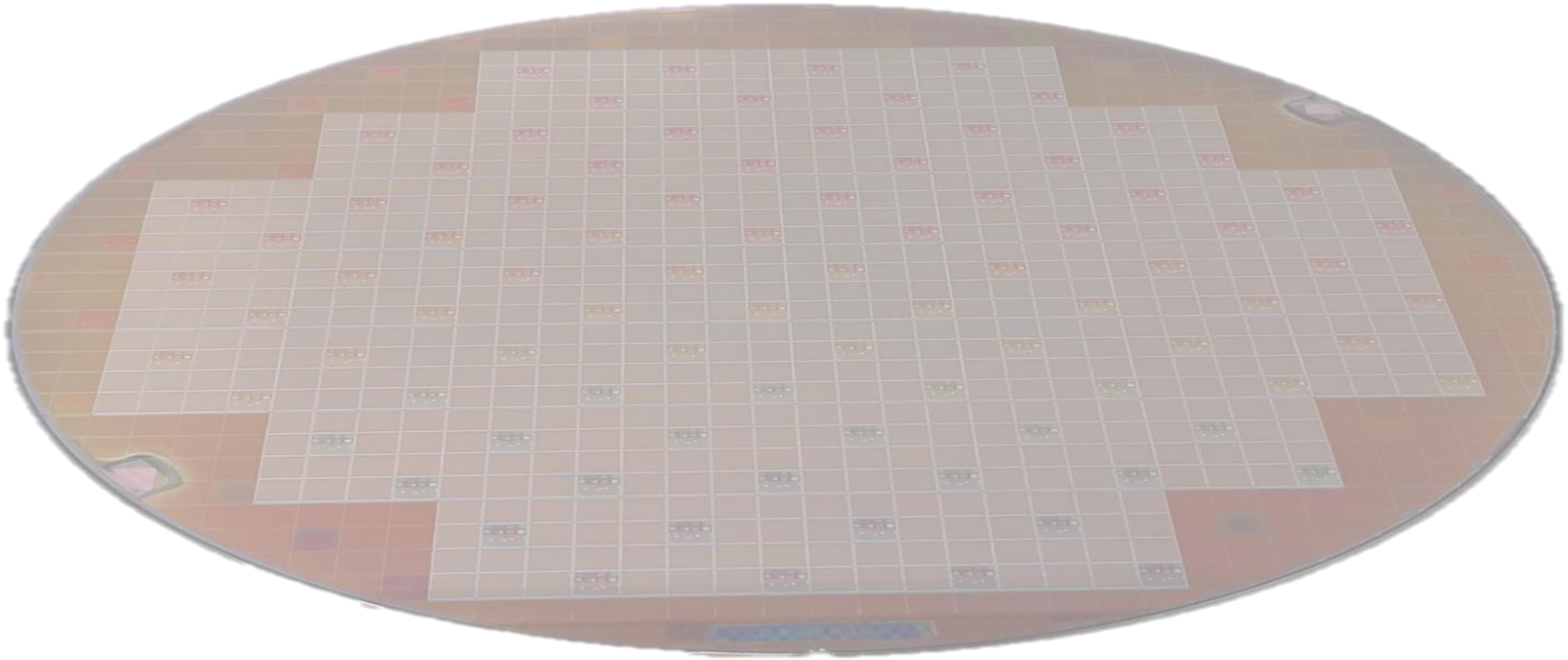
TEST BENCH FOR WAFER-LEVEL MEASUREMENT

Automated movement for wafer-level measurement (over 600 PDC)



Movement of the chuck in relation to the wafer

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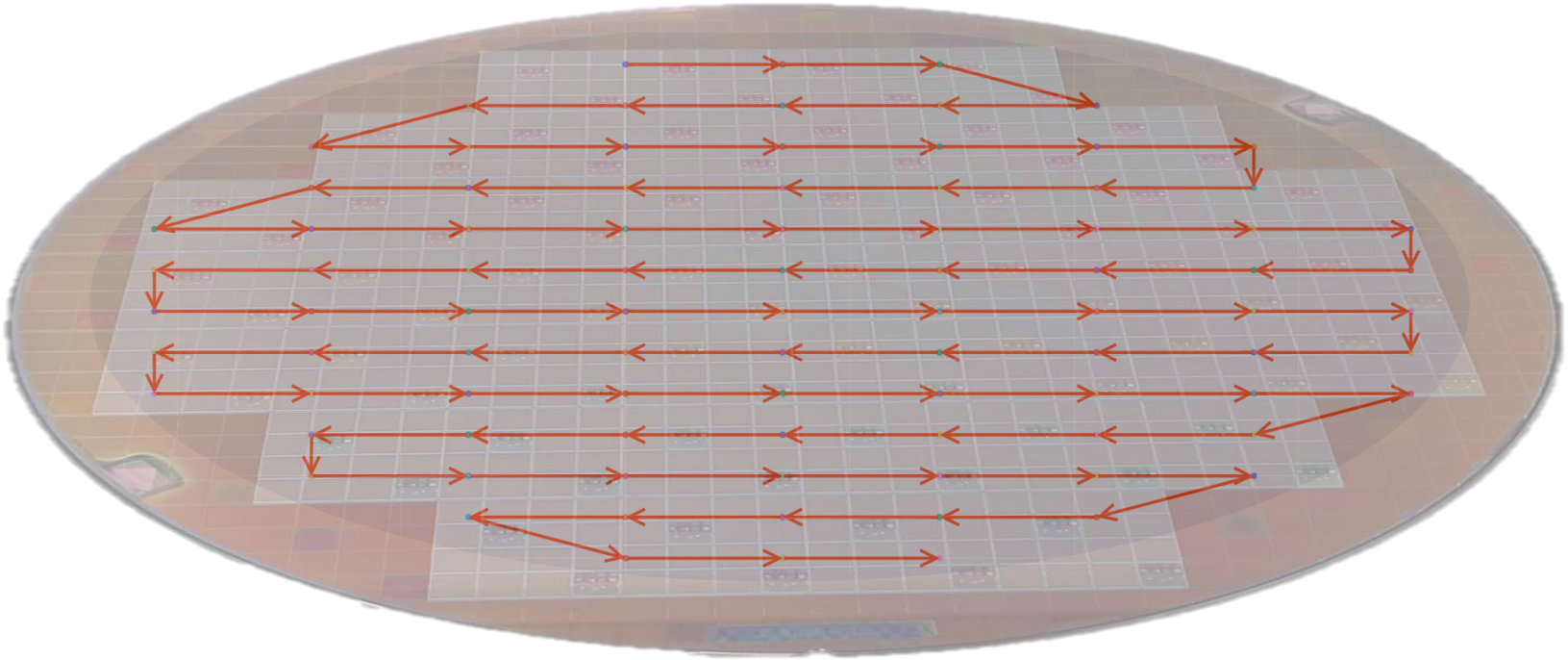
TEST BENCH FOR WAFER-LEVEL MEASUREMENT

Automated movement for wafer-level measurement (over 600 PDC)



Movement of the chuck in relation to the wafer

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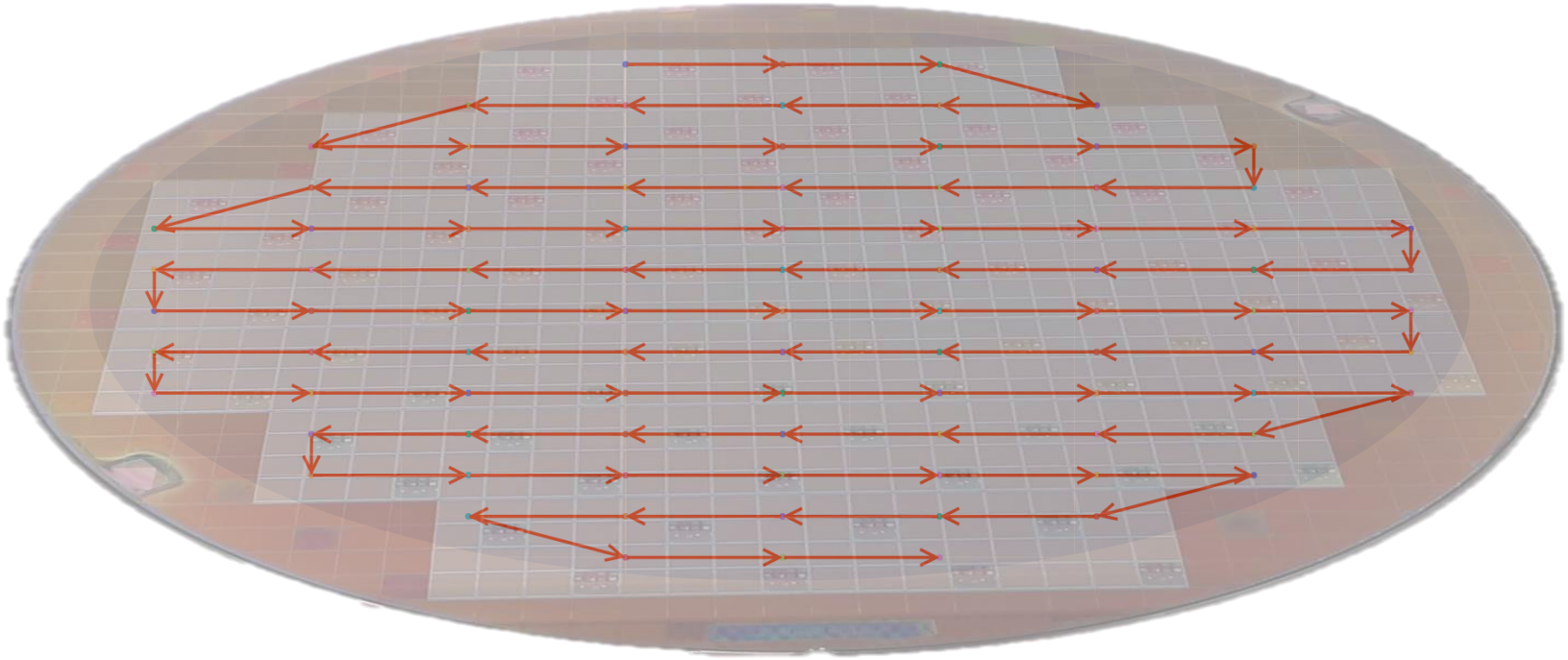
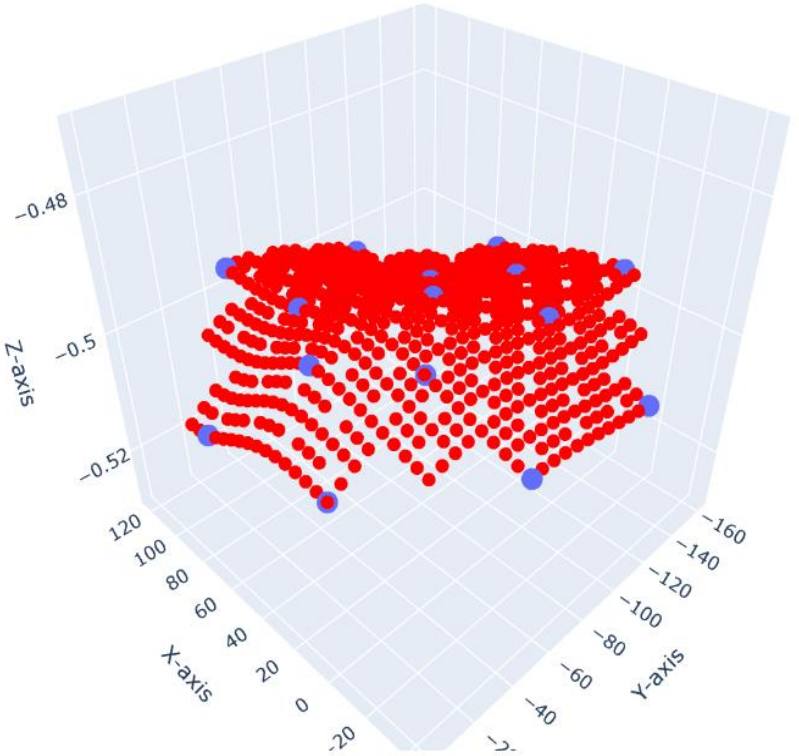


Movement of the chuck in relation to the wafer

Adjusting the height of contact according to wafer topology



Wafer topology

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CONCLUSION

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- Photon-to-Digital Converters keep the information digital all along the acquisition chain.

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- Tile Controller ASIC in development to replace the FPGA boards.

CONCLUSION

- Photon-to-Digital Converters keep the information digital all along the acquisition chain.
- FPGA-based tile controller gives a lot of flexibility to implement multiple features.
  - Flag-based acquisition, dark count mitigation, pulse shape discrimination, and so on.
- Tile Controller ASIC in development to replace the FPGA boards.
- Wafer level measurement will accelerate the testing of multiple PDC for larger system integration.

A TEAM'S WORK

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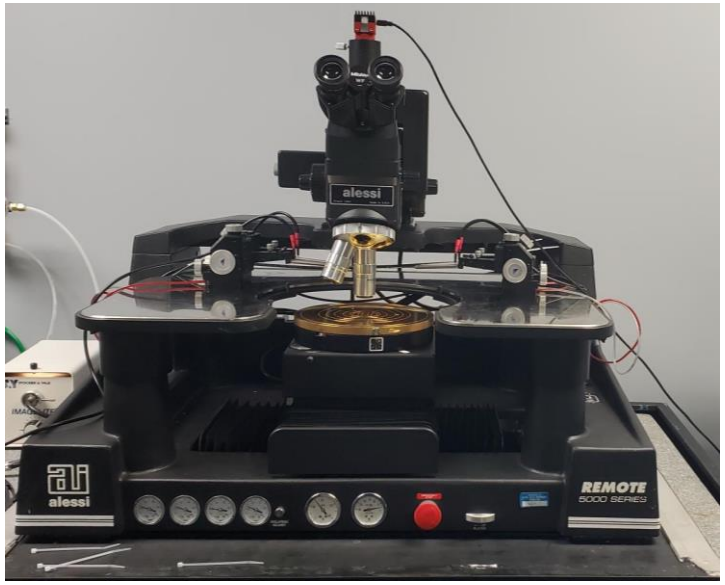
- [1] M. R. Heath *et al.*, "Development of a Portable Pixelated Fast-Neutron Imaging Panel", DOI:10.1109/TNS.2021.3136344.

BACKUP

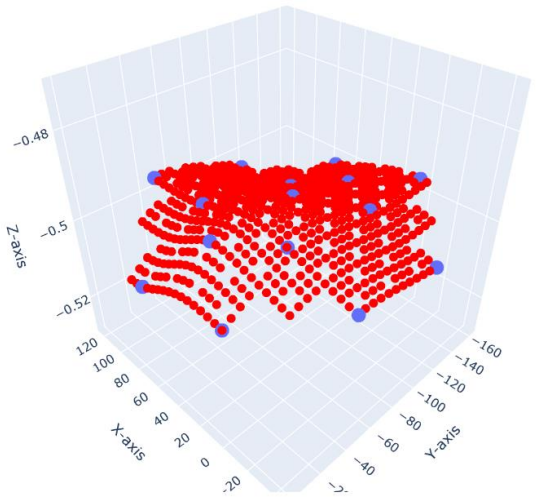
TEST BENCH FOR WAFER-LEVEL MEASUREMENT

Probe station

- Fully automatic chuck enabling scripts for multiple measurement on a wafer
- Program to adapt for the wafer topology



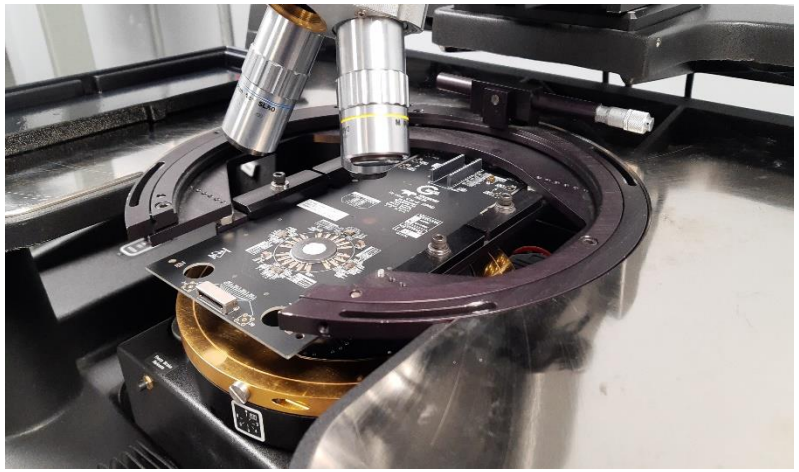
Probe station



Wafer topology

Probe card

- Can act as the interface between the PDC and the controller (FPGA)



Probe card on the station

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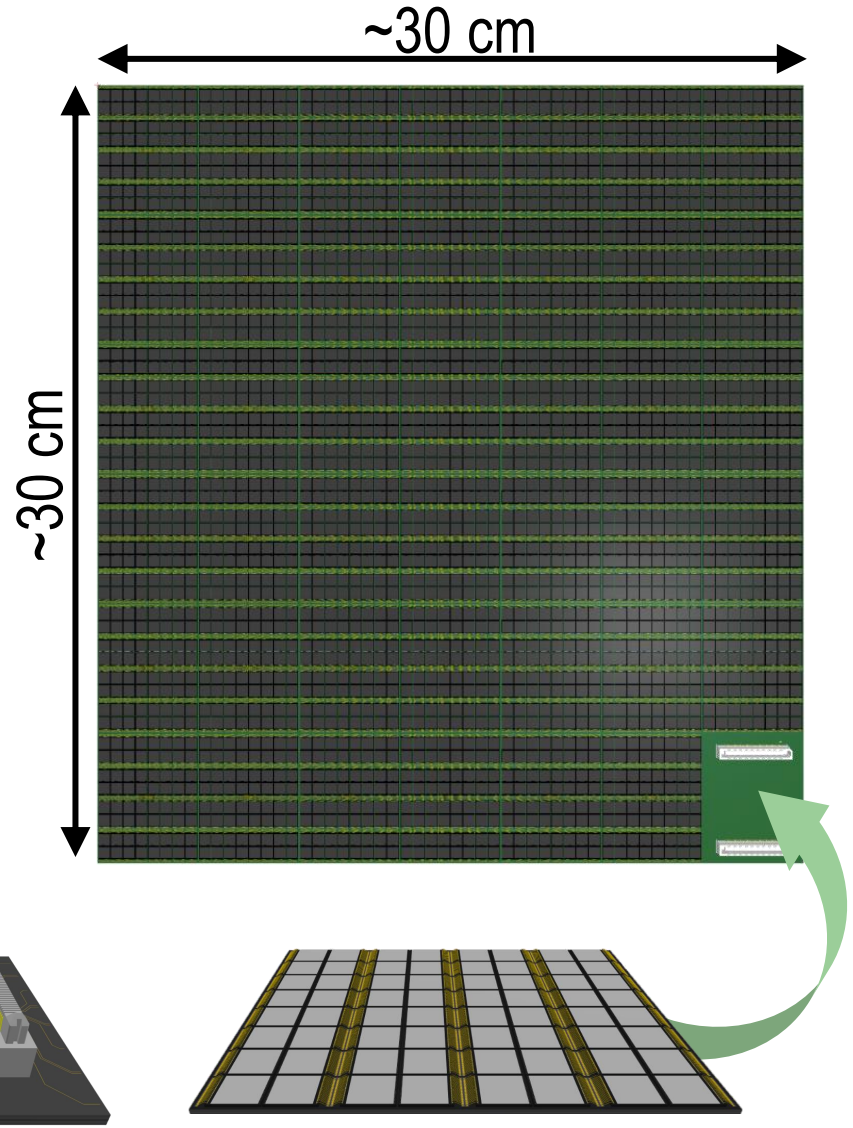
PORTABLE API-BASED NEUTRON RADIOGRAPHY

- PDC panel array of 42 modules of 8 x 8 PDC
- 400-500 nm peak pixelated plastic scintillators
- 11E+6 SPADs over 30 x 30 cm^2
- 40W PDC power consumption
  - 10 ns binning for 3k events/s/PDC,
  - 128 bins/event (1280 ns range/event)
- Simulated timing distribution PDC of 25 ps RMS



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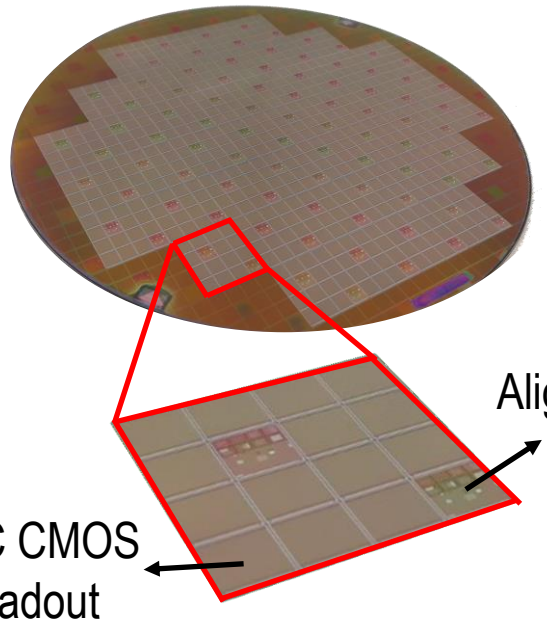
DIGITAL SOLUTION: TOWARDS A 3D INTEGRATION

8 inch CMOS wafer

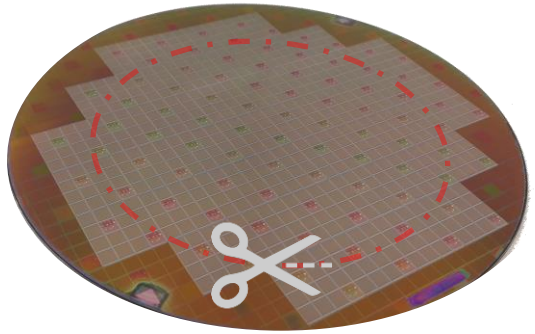


Alignment die for 3D bonding

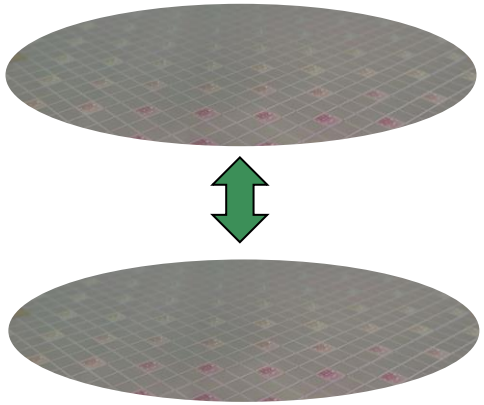
PDC CMOS readout

Reticle of 4 × 4 dies

8 inch to 6 inch coring down



3D Bonding @ Teledyne DALSA (TDSI)

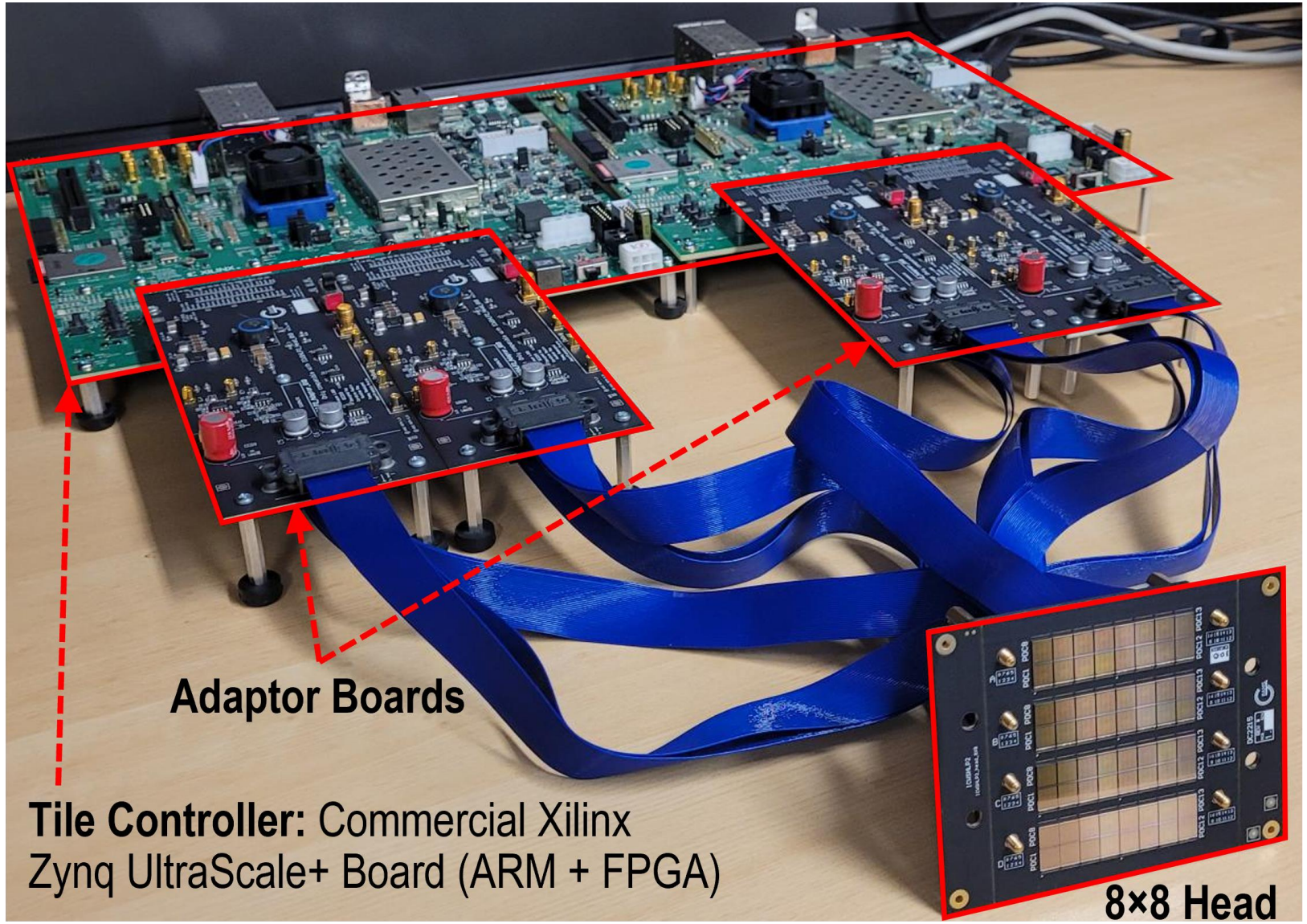


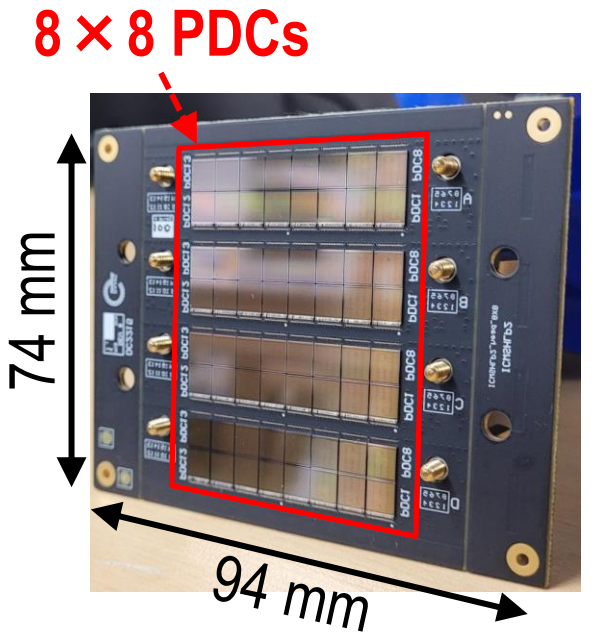
6 inch **SPAD wafer**

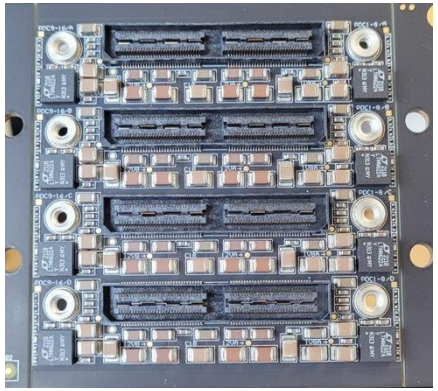
6 inch **CMOS wafer**

*SPAD process & 3D bonding process completed @ TDSI

8 × 8 PHOTODETECTION MODULE







8 × 8 PCB tile prototype

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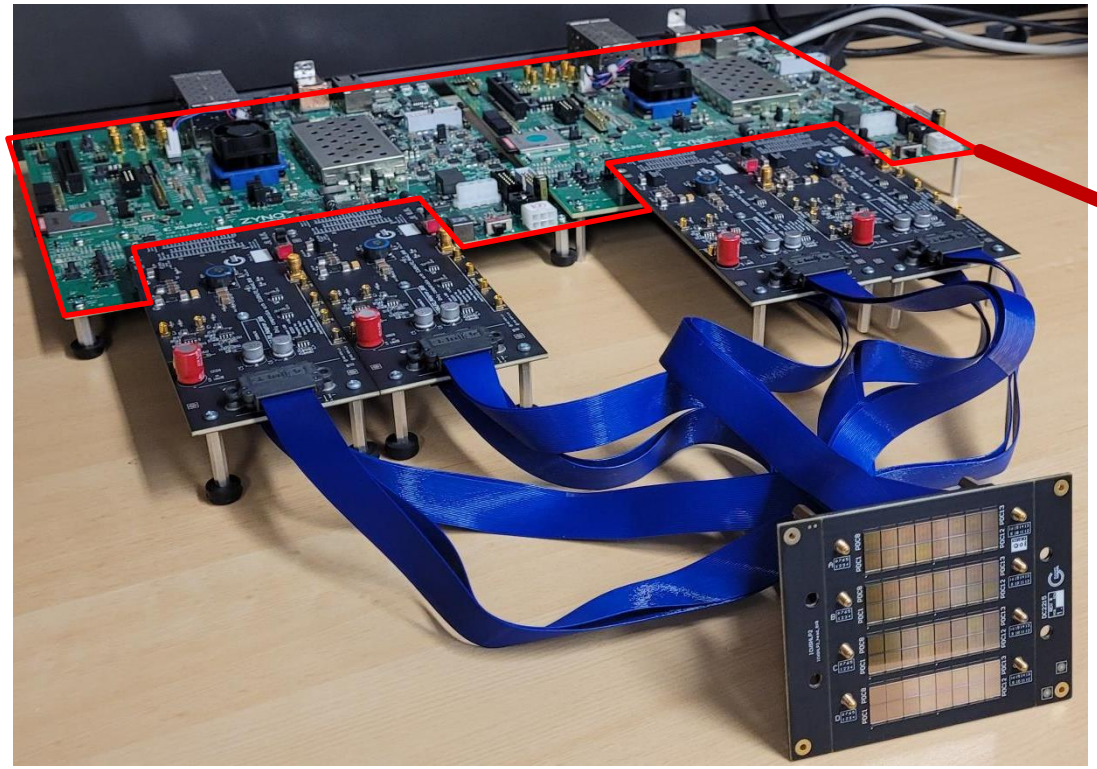
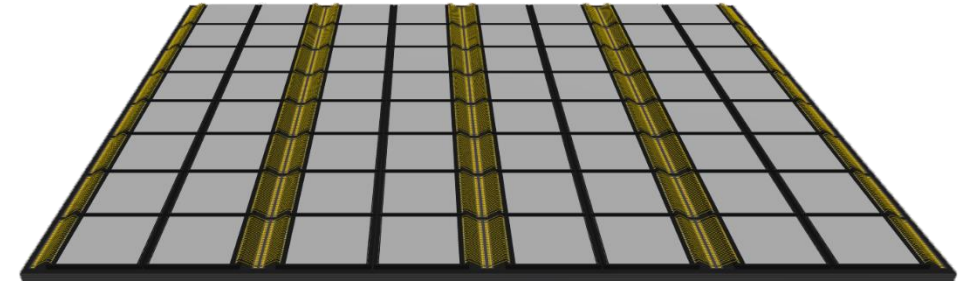
NEXT STEP: FPGA BOARD TO A TILE CONTROLLER

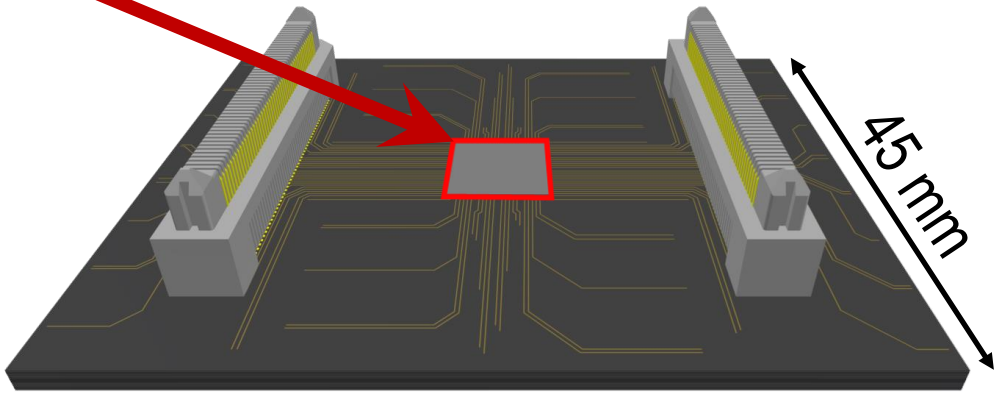
FPGA-based Controller



ASIC-based Controller



Top side



Bottom side

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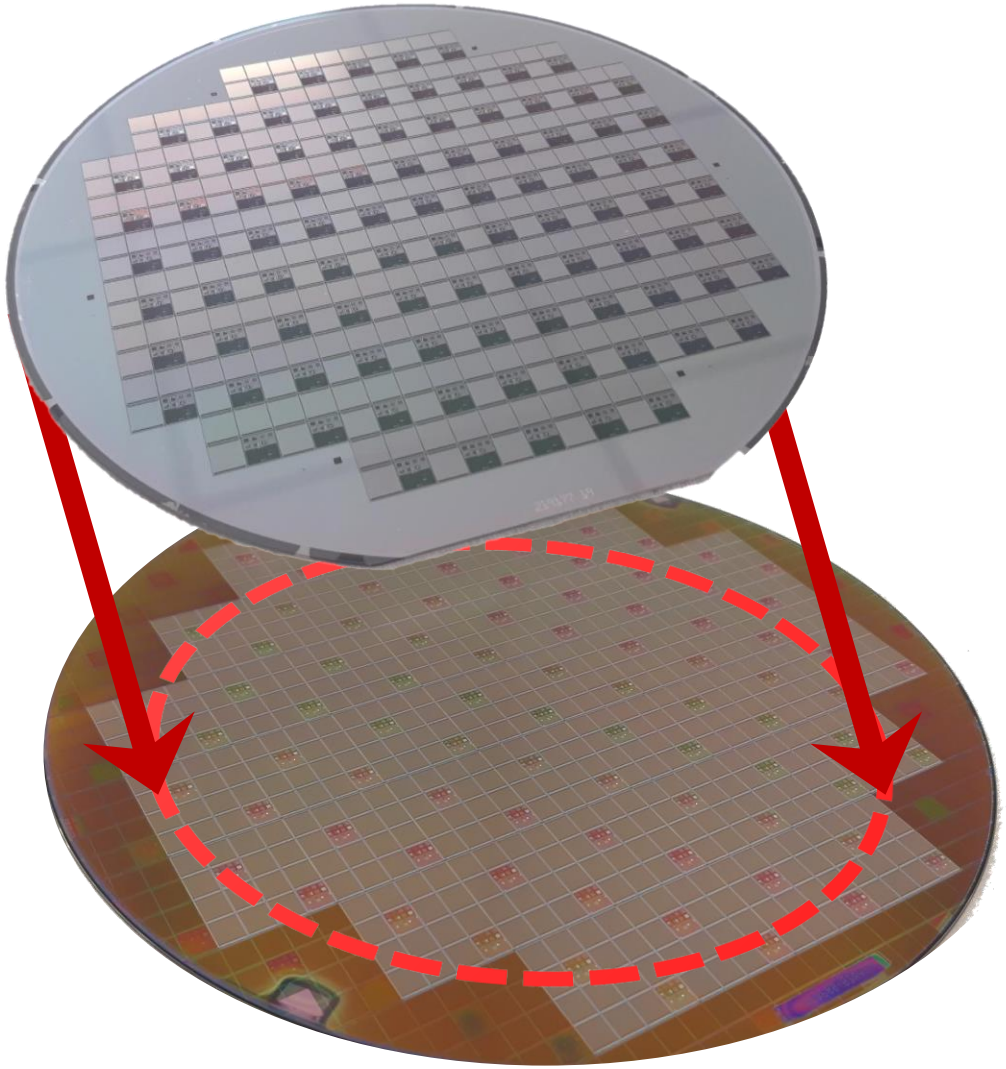
TOWARD 3D-PDC

150 mm SPAD wafer



200 mm PDC wafer

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