

# Photon-to-Digital Converter for Large Scale Noble Liquid Detectors

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SPAD array-based photodetectors are emerging in large-scale photodetector panels because of their appealing characteristics such as compactness, low bias voltages and good photon detection efficiency (PDE). Conventional SiPMs are considered for covering large areas, but the large capacitance of SiPMs brings a serious limitation. They also require an analog readout circuit designed with tradeoffs between power consumption, bandwidth and noise.

To overcome some of the SiPM challenges, this paper presents a photodetection module populated with photon-to-digital converter (PDC) CMOS readout ASICs and tailored for thousands of  $\text{cm}^2$  up to  $\text{m}^2$  panels. The prototype that will be presented is a  $94 \times 74 \text{ mm}^2$  module assembled with  $8 \times 8$  PDC readout ASICs. Each ASIC has 4096 individual SPAD readout circuits at  $78 \mu\text{m}$  pitch distributed over a  $5 \times 5 \text{ mm}^2$  area. Each of the 64 ASICs is connected to a tile controller implemented on an external FPGA platform to demonstrate the readout architecture. The tile controller is used to configure, program the PDC bin width (from 10 ns up to  $\mu\text{s}$ ) for photon counting and send the bin counts to a computer to visualize the data.

The tile controller can implement pulse shape discrimination, dark count mitigation, and time-to-digital converters with sub 100 ps timing resolution. These have been demonstrated on a preliminary  $2 \times 2$  PDC readout ASIC module. We will also discuss the latest measurements on the  $8 \times 8$  PDC tile.

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