

Single-photon avalanche diodes VUV enhancement for fundamental physics experiments

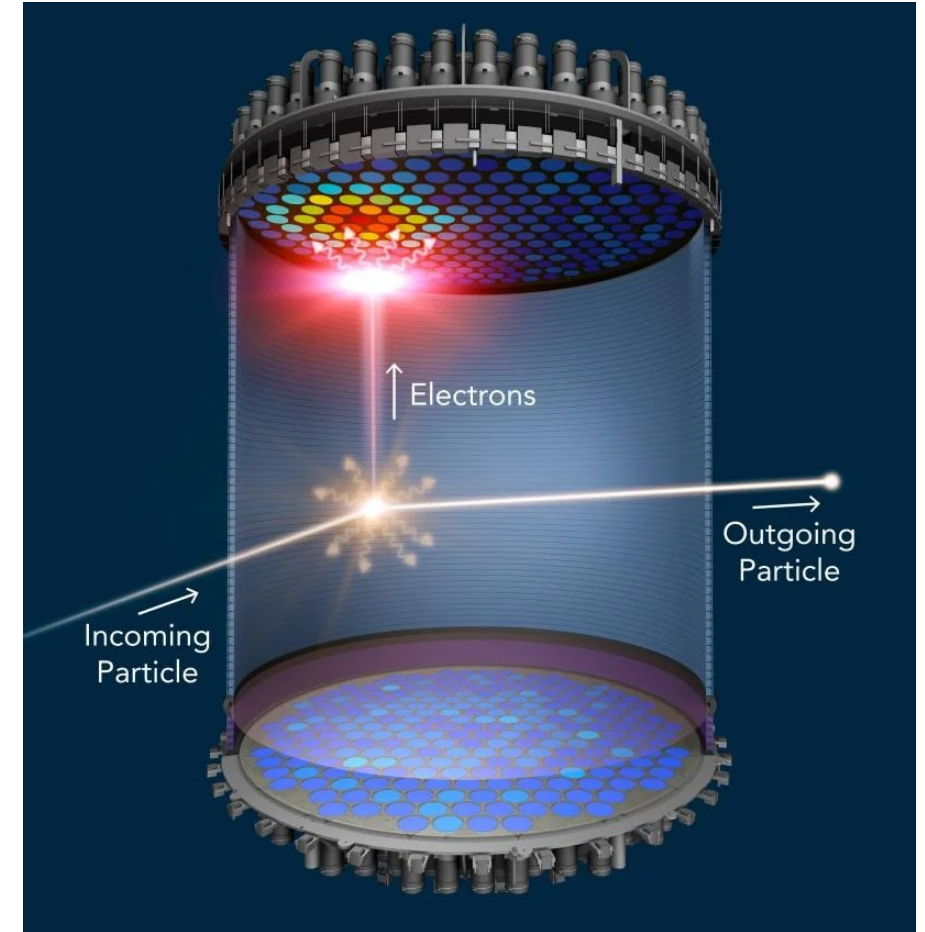
J. Deshaies^{a+}, C. Tindall^b, F. Vachon^a, A. Turala^a, C. M. Pepin^a, P. Denes^b, F. Retiere^c,
J.F. Pratte^a, A. Boucherif^a, S. A. Charlebois^a.

17/02/2024



Time projection chamber (TPC) experiments ($0\nu\beta\beta$, dark matter)

- TPC are widely used in dark matter and neutrino experiments
- γ scintillation used to position events and time-stamps events
- Spatial resolution is essential discern meaningful events from background rad

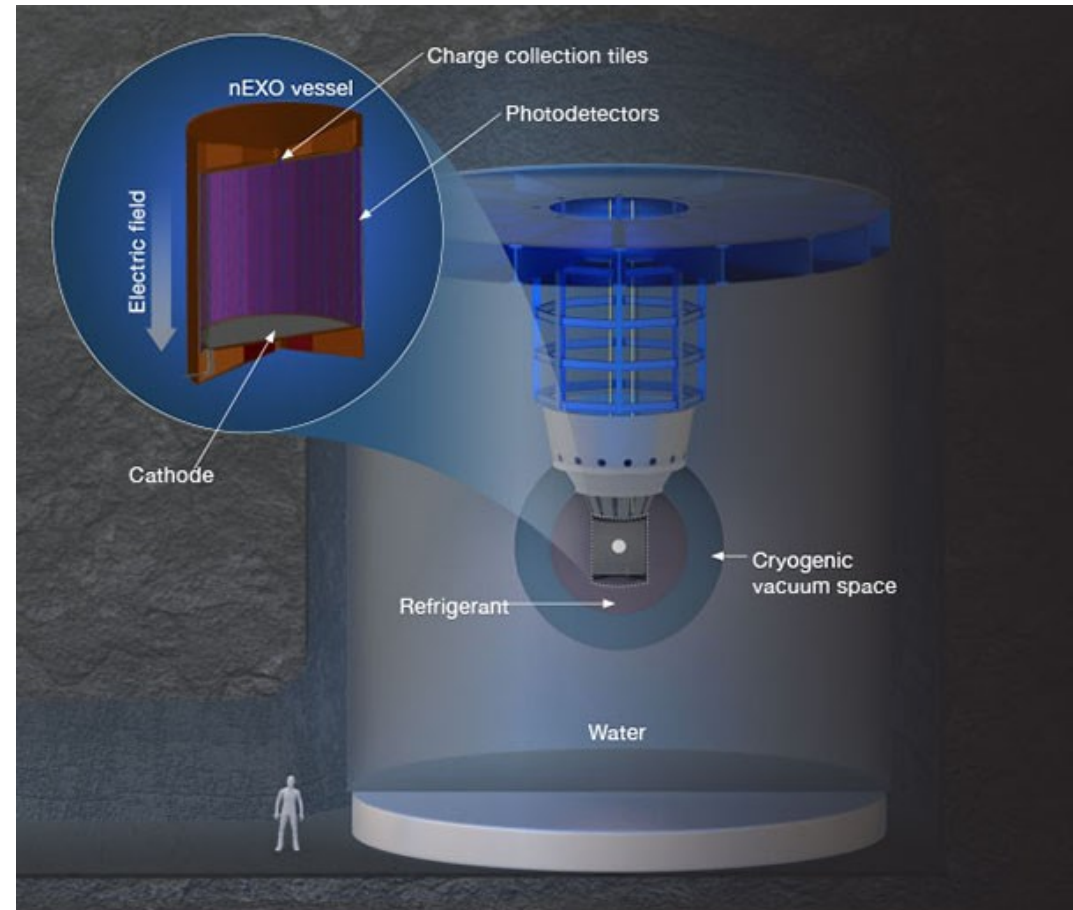


LUX-Zeplin LZ detector
(SLAC National Accelerator Laboratory)

Xe scintillation based neutrinoless $0\nu\beta\beta$ experiments (nEXO, NEXT)

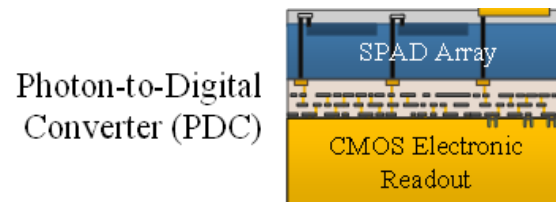
Caio Licciardi's talk from Friday

- $0\nu\beta\beta$ detection is rare and highly sensible to noise ($0\nu\beta\beta$ vs $2\nu\beta\beta$ vs background)
- Small gain in detection efficiency = years' worth of data collection
- No commercial solutions designed specifically (ground up) for physics experiments requirements (low rad, noise and high det %)



Photon detector module (PDM) requirements for $0\nu\beta\beta$ experiments

- Sherbrooke set themselves to the task of designing PDMs optimized for physics requirements



- Olivier's talk on Friday (#133)
- Higher PD efficiency is main goal**

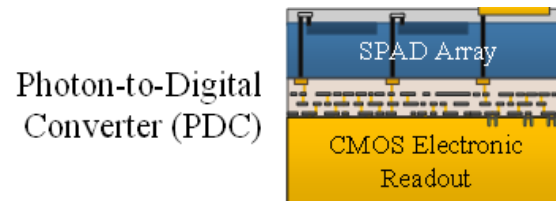
TABLE I
SUMMARY OF SiPM PARAMETERS REQUIRED BY NEXO. PARAMETERS IN ITALIC ARE PREFERABLE, BUT NOT MANDATORY.

Parameter	Value
Photo-detection efficiency at 175-178 nm (without anti-reflective coating in gas/vacuum)	$\geq 15\%$
Radio-purity: <i>^{232}Th and ^{238}U</i>	$< 10 \mu\text{Bq/kg}$
Dark noise rate at -100°C	$\leq 50 \text{ Hz/mm}^2$
After-pulse and cross-talk probability	$\leq 20\%$
Single photodetector active area	$\geq 1 \text{ cm}^2$
<i>Gain fluctuations and electronic noise</i>	$\leq 0.1 \text{ p.e.}$
<i>Single photon timing resolution</i>	$< 10 \text{ ns}$

I. Ostrovskiy, Characterization of Silicon Photomultipliers for nEXO, 2015.

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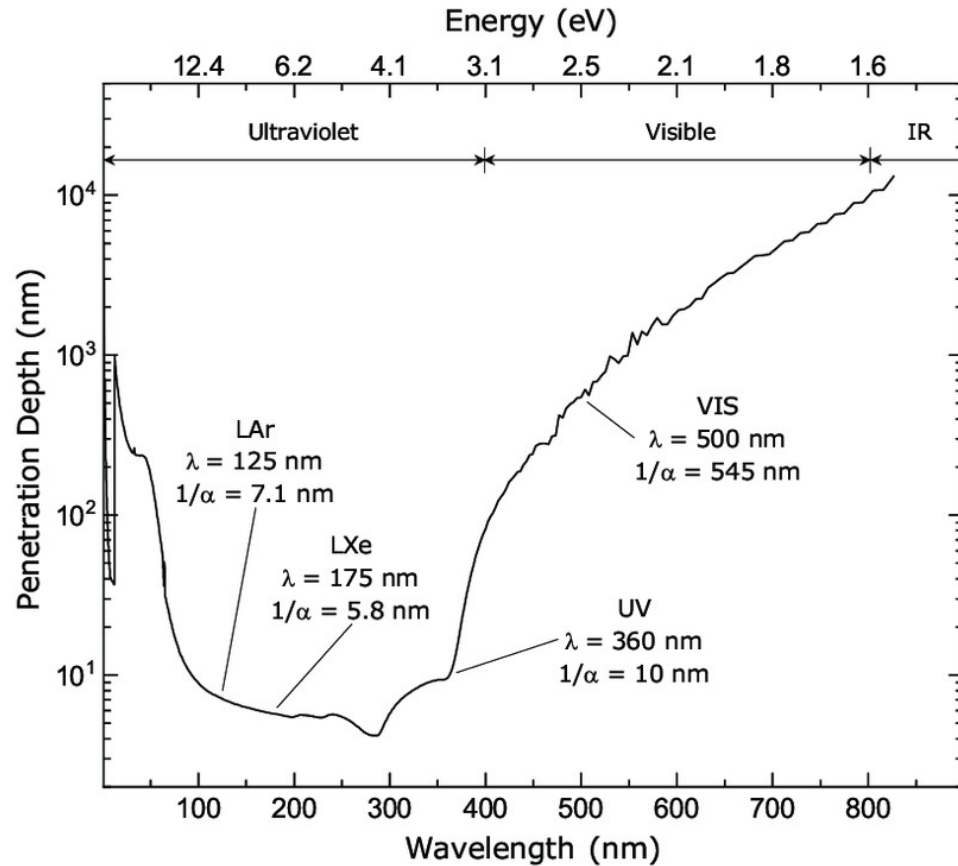
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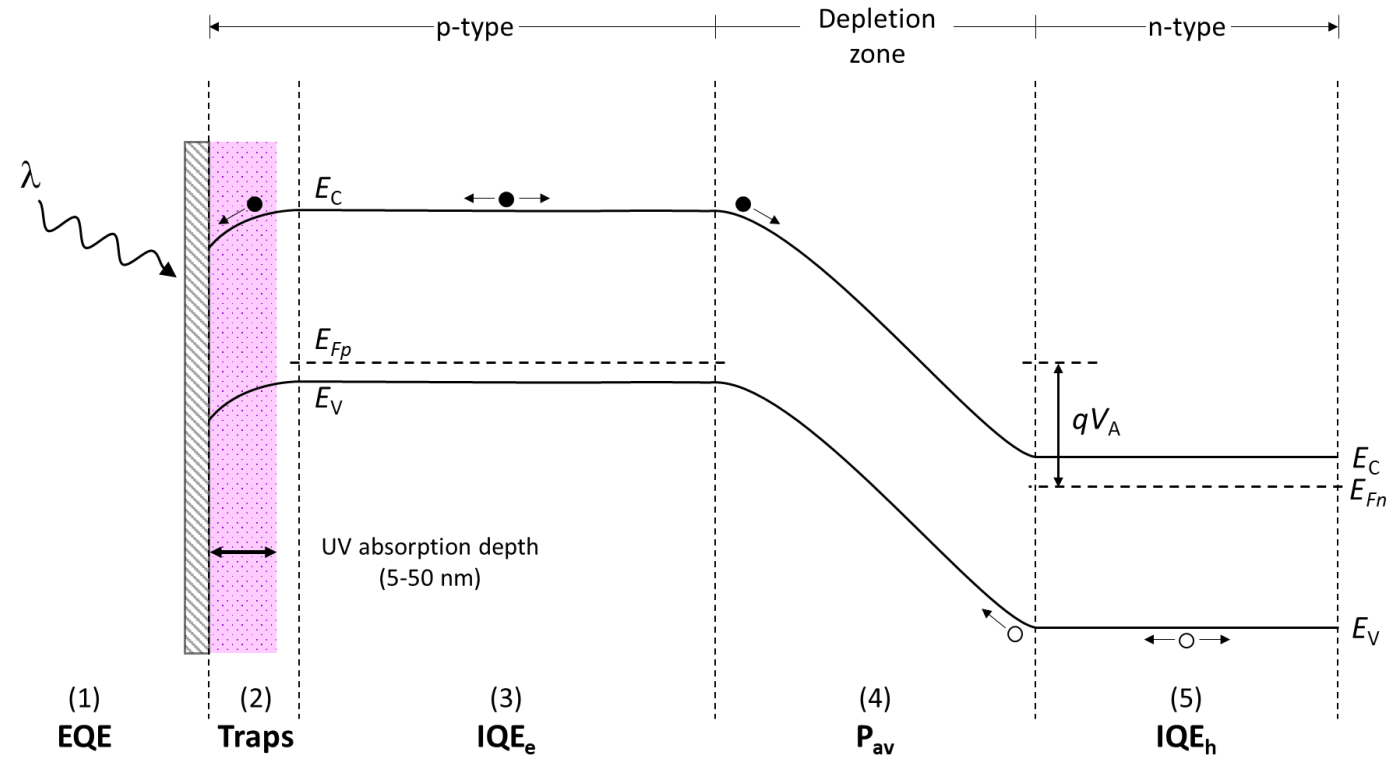
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Silicon based devices sensitivity in UVs

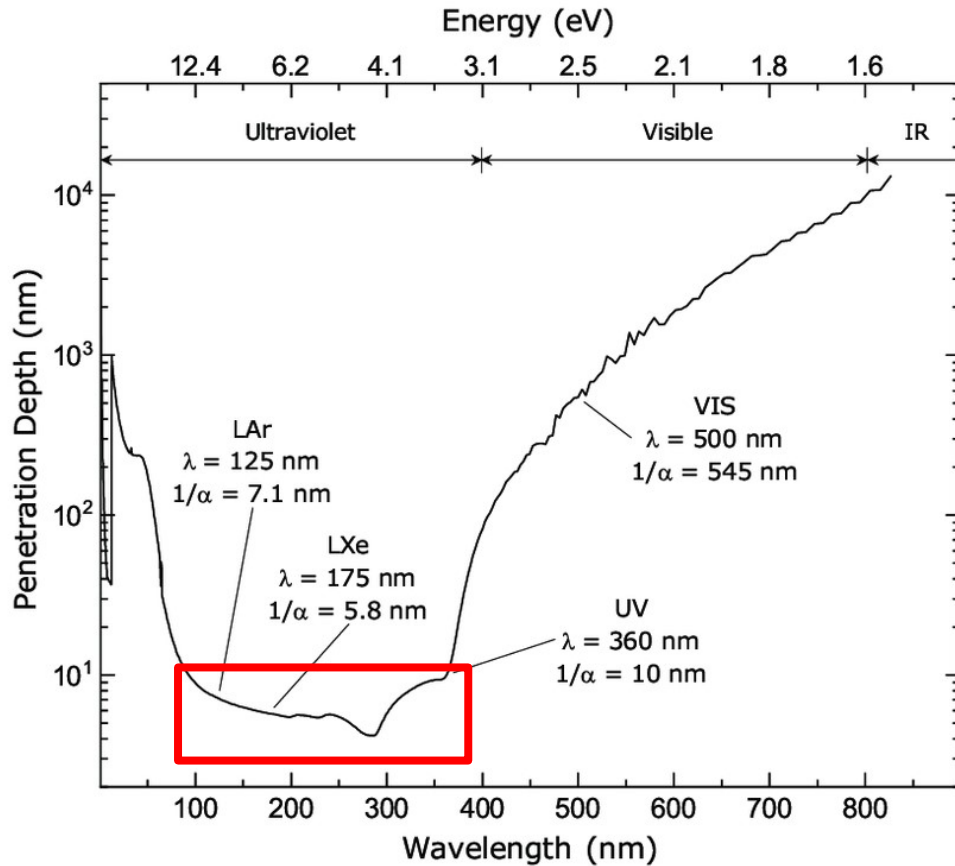


Pratte, JF. 3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works 2021

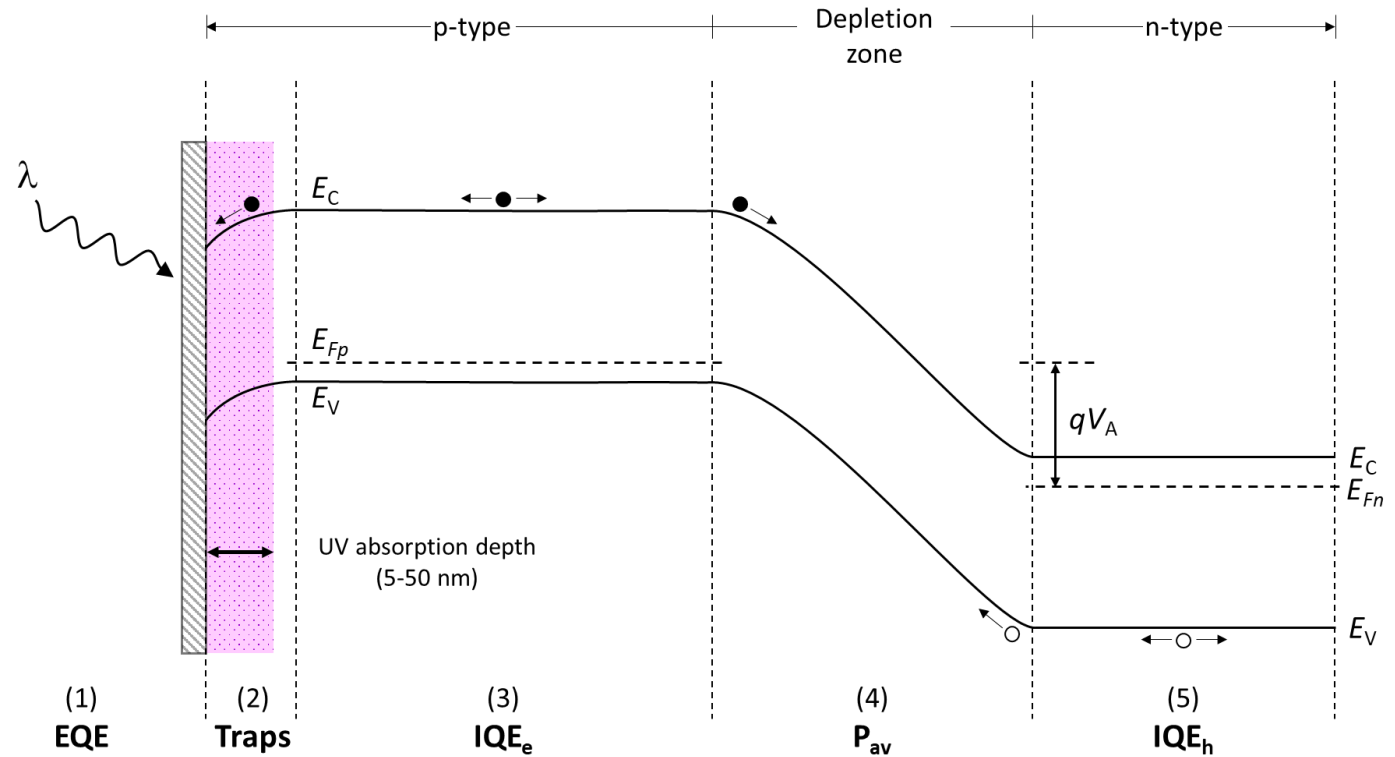


F.Vachon, Masters thesis, Université de Sherbrooke, 2021.

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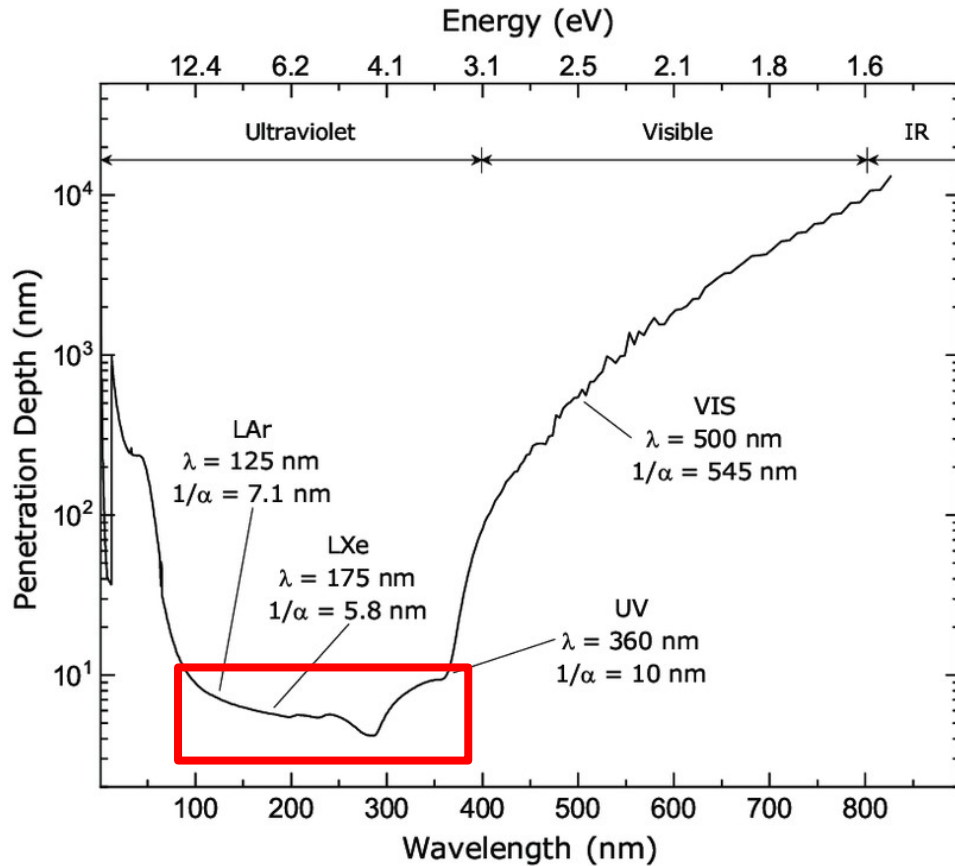


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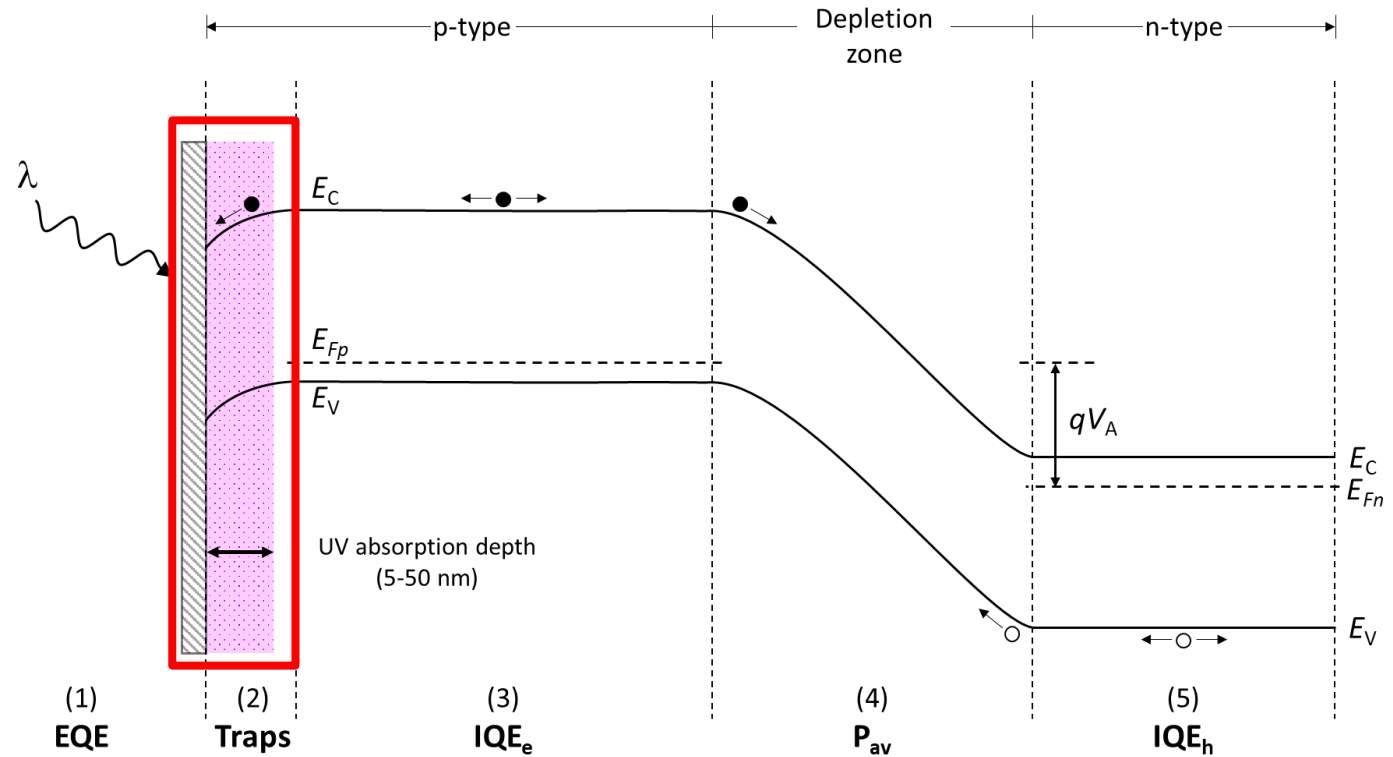


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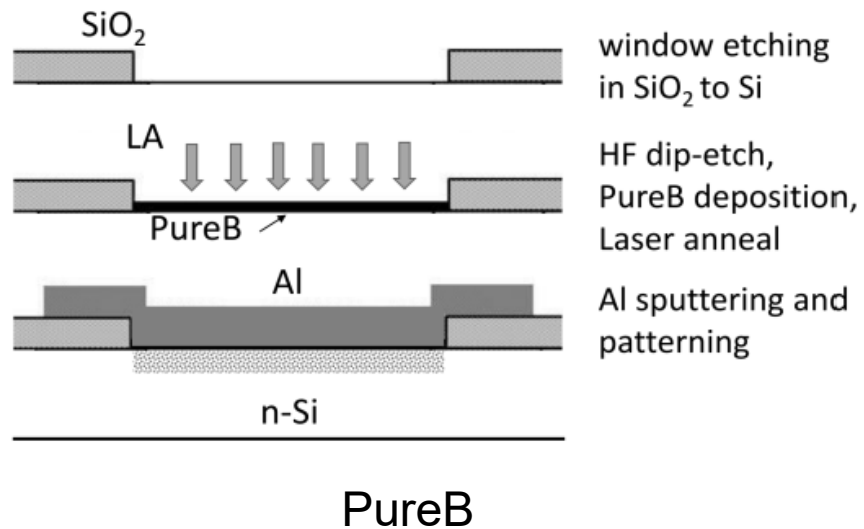
Pratte, JF. 3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works 2021



F.Vachon, Masters thesis, Université de Sherbrooke, 2021.

UVs enhancement techniques

- Reducing surface potentials effect (IQE)



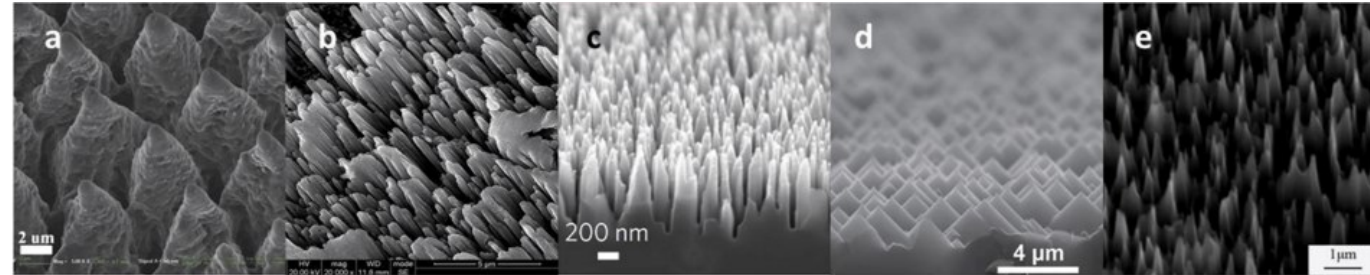
window etching
in SiO₂ to Si

HF dip-etch,
PureB deposition,
Laser anneal

Al sputtering and
patterning

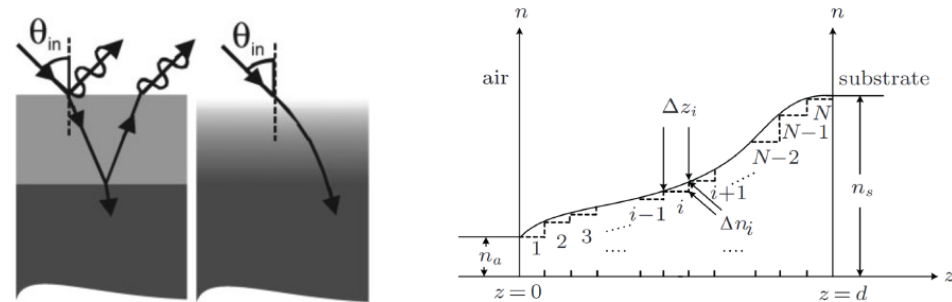
L. Nanver, An experimental view on PureB silicon photodiode device 2018

- Improving transmission (EQE)



Black silicon

Zheng Fan, Recent Progress of Black Silicon: From Fabrications to Applications 2020

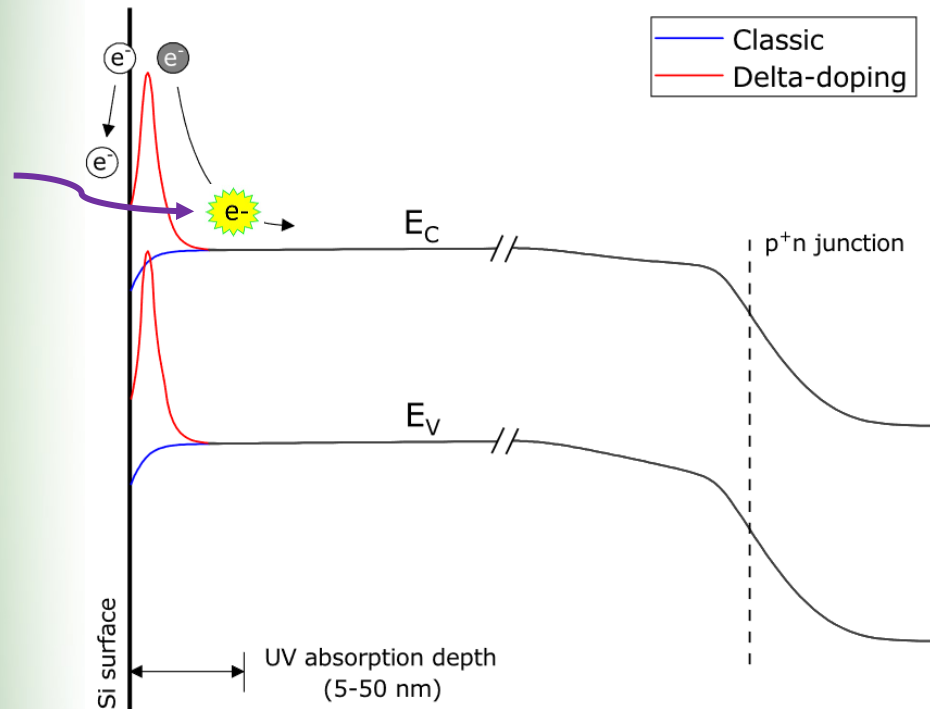


GRIN-ARC & 1/4-ARC

Silke L. Diedenhofen, Broad-band and Omnidirectional Antireflection Coatings Based on Semiconductor Nanorods, 2009

Delta doping (IQE)

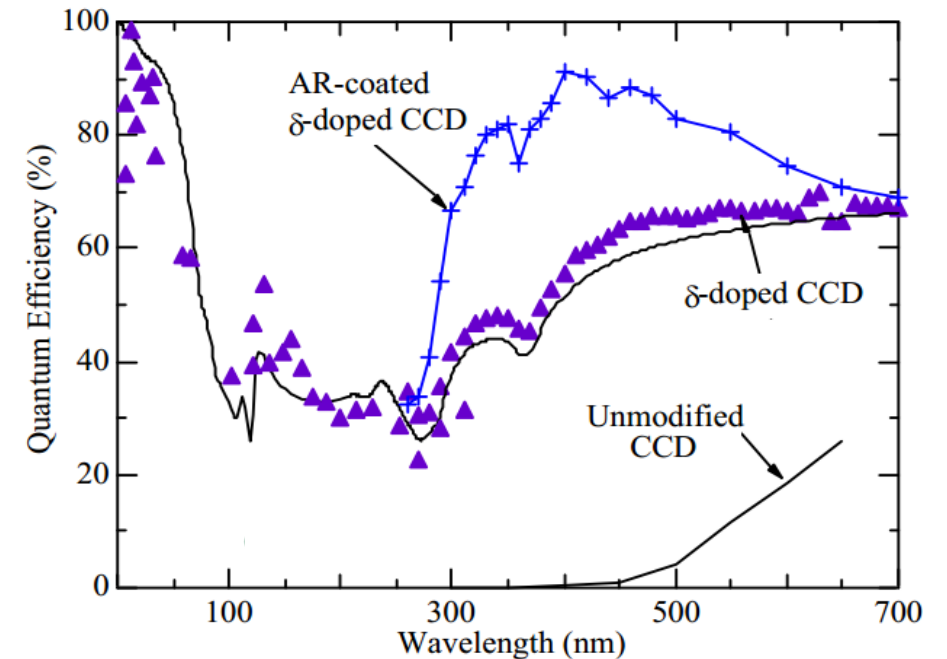
- Sharp peak of dopant (boron) “pushes” minority carriers either toward depletion zone or surface



F.Vachon, Masters thesis, Université de Sherbrooke, 2021

- JPL 1992 molecular beam epitaxy (MBE) grown δ -doped layer on backside illuminated CCDs restored unity IQE

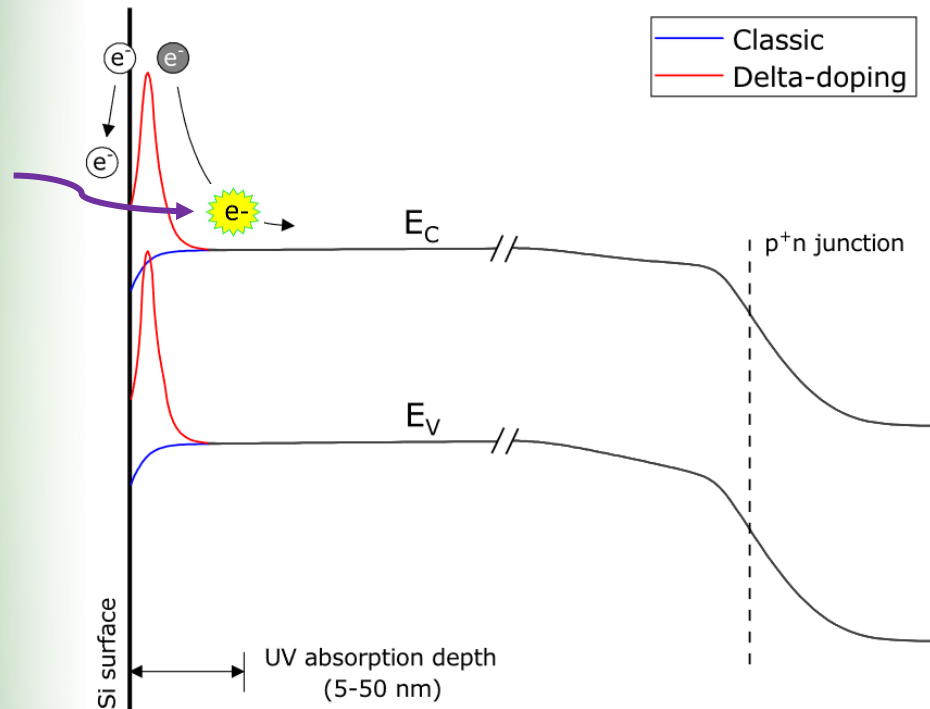
Quantum efficiency of “ δ -doped CCDs”



Growth of a delta-doped silicon layer by molecular beam epitaxy on a charge-coupled device for reflection-limited ultraviolet quantum efficiency. M.E. Hoenk et al. Applied Physics Letters 61, no. 9 (1992): 1084-1086.

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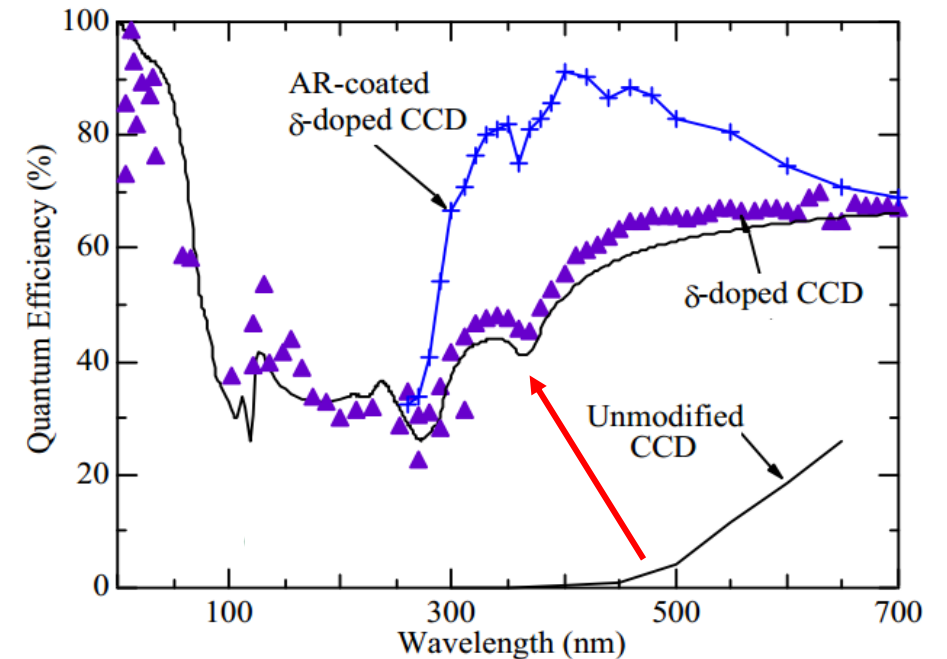
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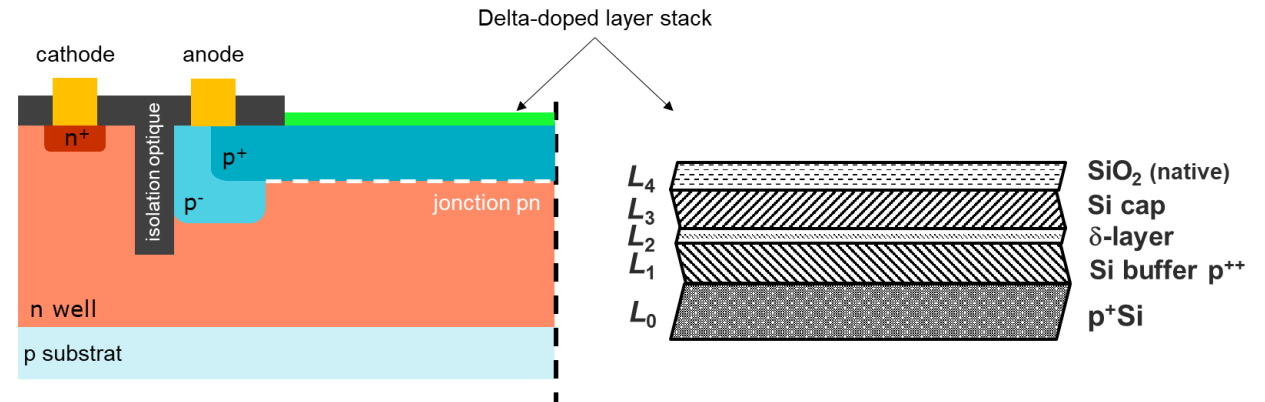


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UdeS delta layer - detail

Layer (inspired by JPL) designed for $\lambda = 175$ nm (LXe scintillation):

- 4 nm p⁺⁺ (Si-B) (L1)
- 4 ML Boron (L2)
- 4 nm Si cap (L3)



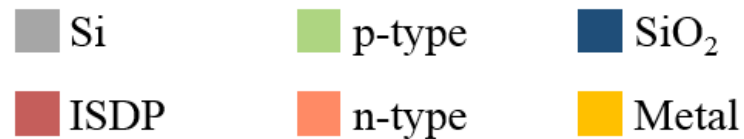
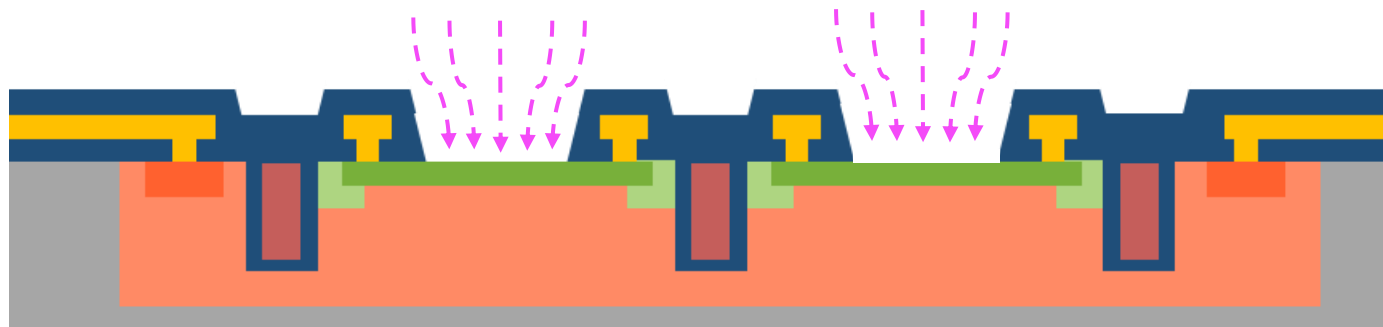
Details of the δ -doped layer developed by Frederic Vachon for nEXO experiment

F.Vachon, Masters thesis, Université de Sherbrooke, 2021.

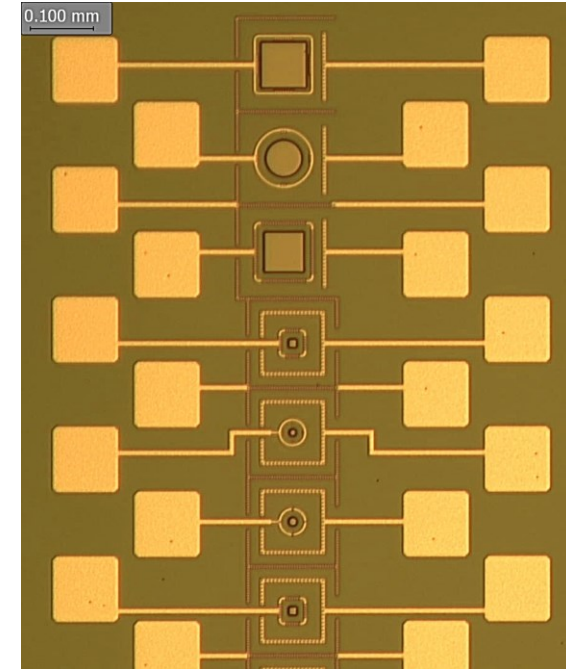
Grown by MBE for thickness and doping precision

Growth on device: process limitation(s)

- Al contact pads and rings low diffusion T° (450°C) (spiking)
- Epitaxy on metal + oxide (frontside) patterned surface complexifies chemical cleaning (RCA, HF)



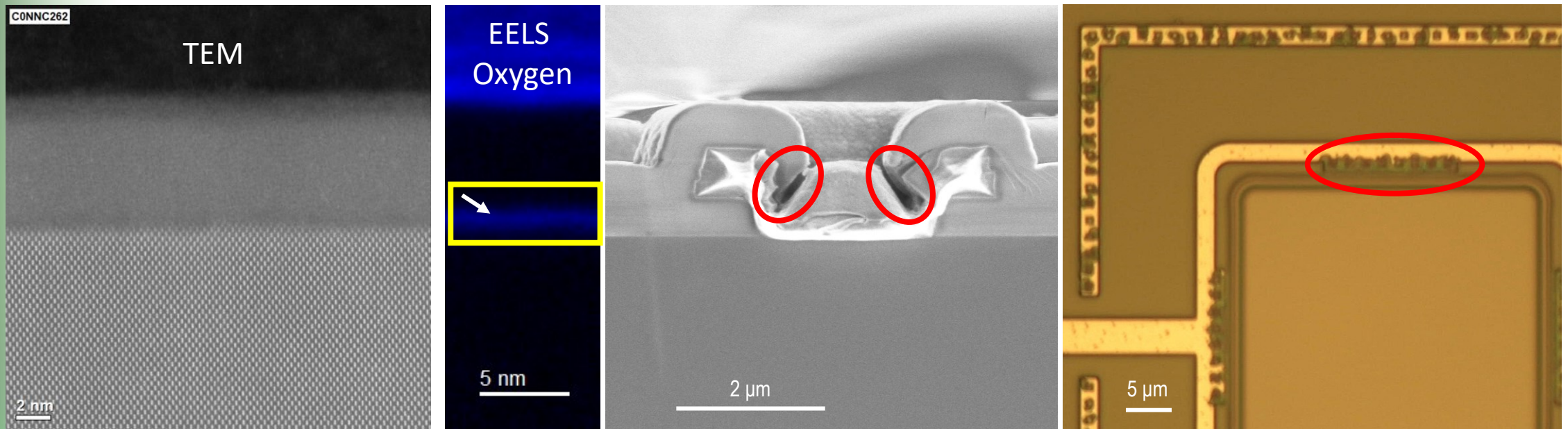
F.Vachon, Masters thesis, Université de Sherbrooke, 2021.



2D SPAD array test structure

MBE surface preparation and prior results

- State of the art Low-Temperature (LT) MBE insufficient for our application
- Runs at *Lawrence Berkeley National Lab (LBNL)* prior to project led to amorphous growths (SiO_2 interface), and **reduced photodetection efficiency**



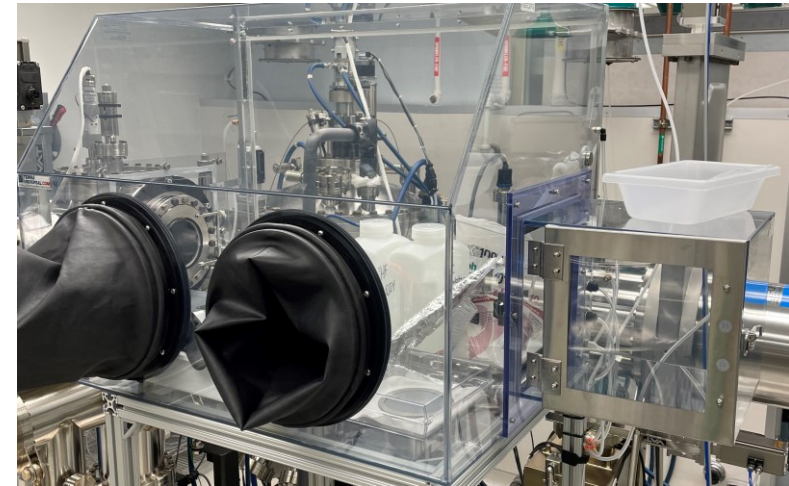
Updated process

Goals

1. Eliminate **close to all oxide** while minimizing surface roughness
2. Minimize thermal budget to **maintain device integrity**
3. **Enable crystalline growth of Si**

Solution

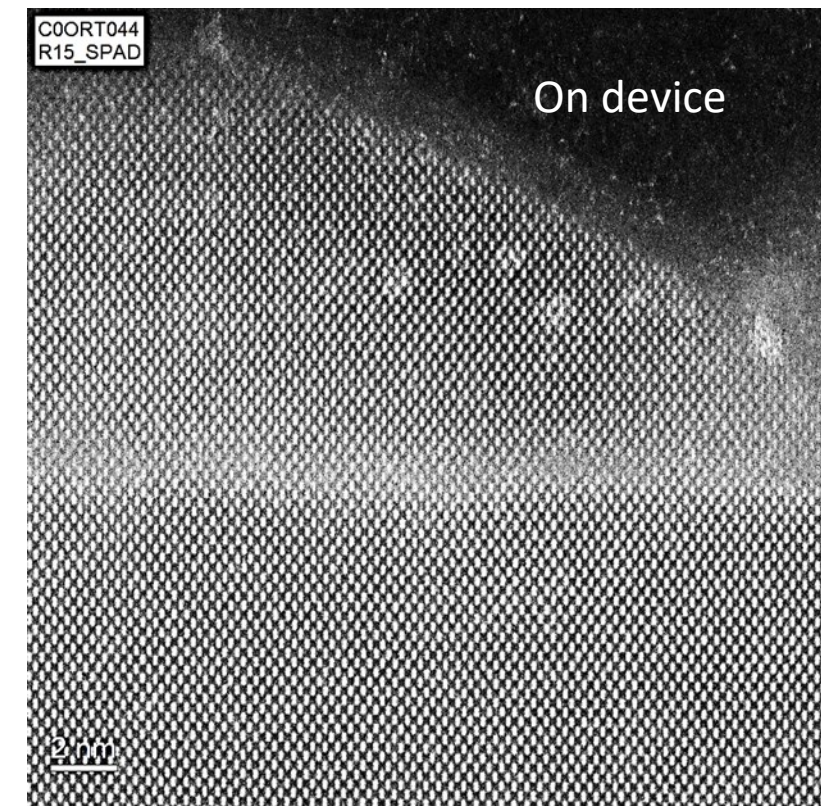
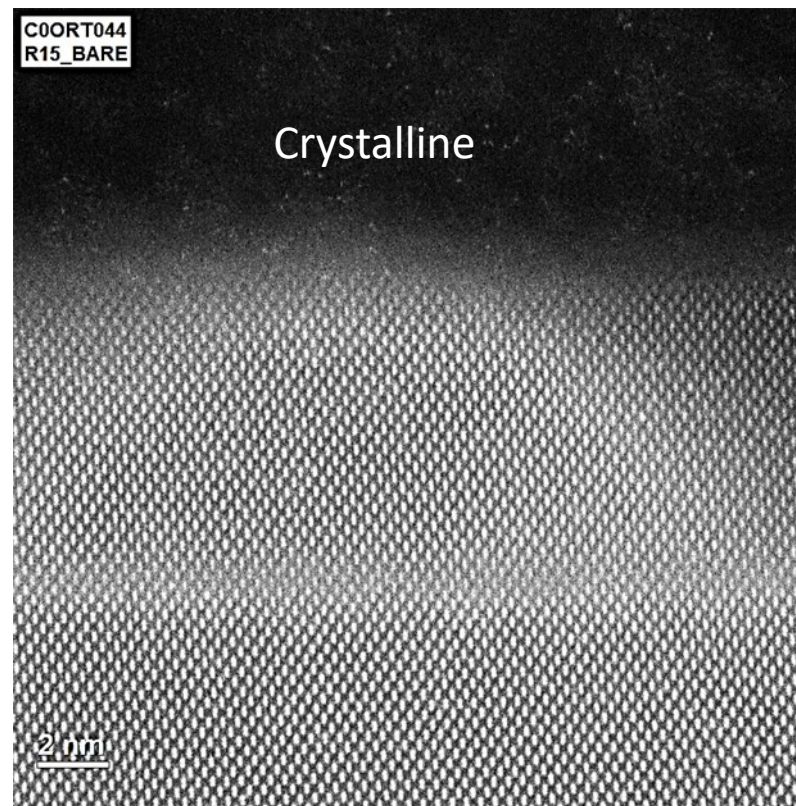
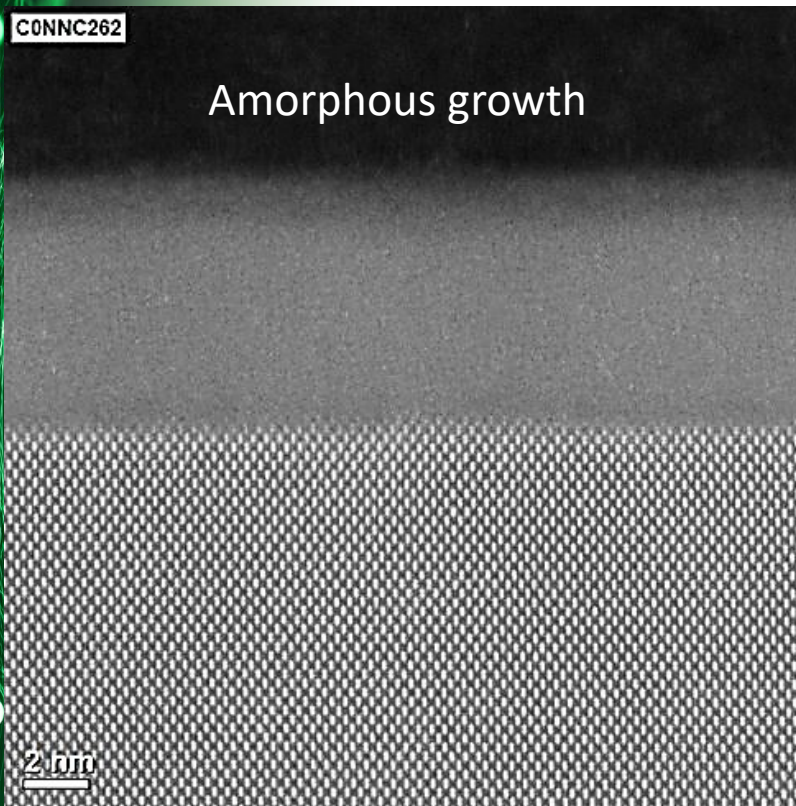
- **Addition of a glovebox on reactor** (cleaning in N purged environment)
- **Dual cleaning:** BOE 6:1 + surfactant (rough) followed by HF 1% (flatten)



Glovebox on LBNL reactor

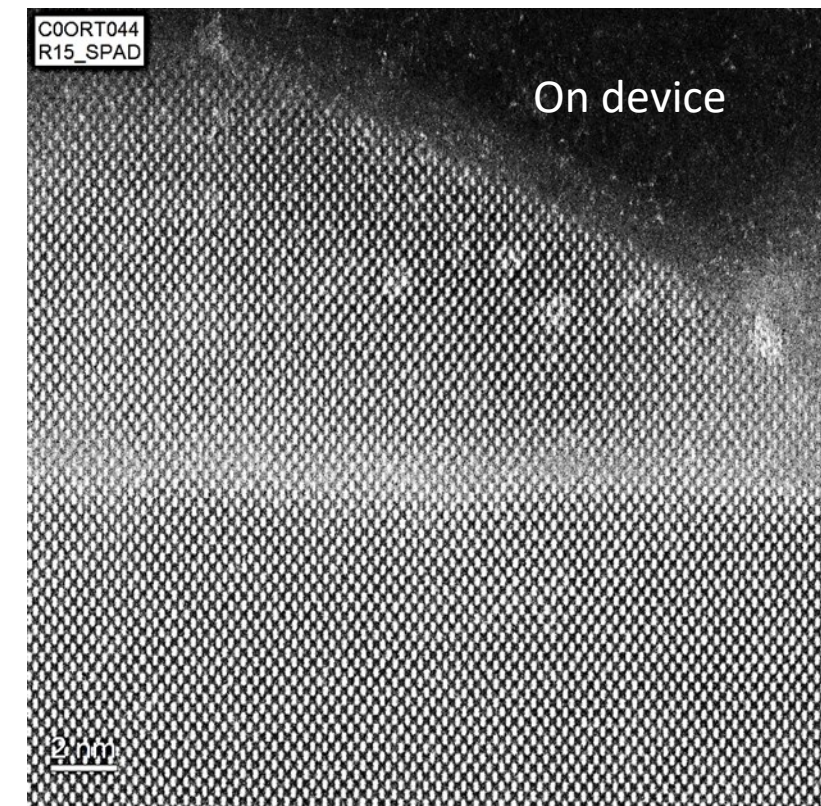
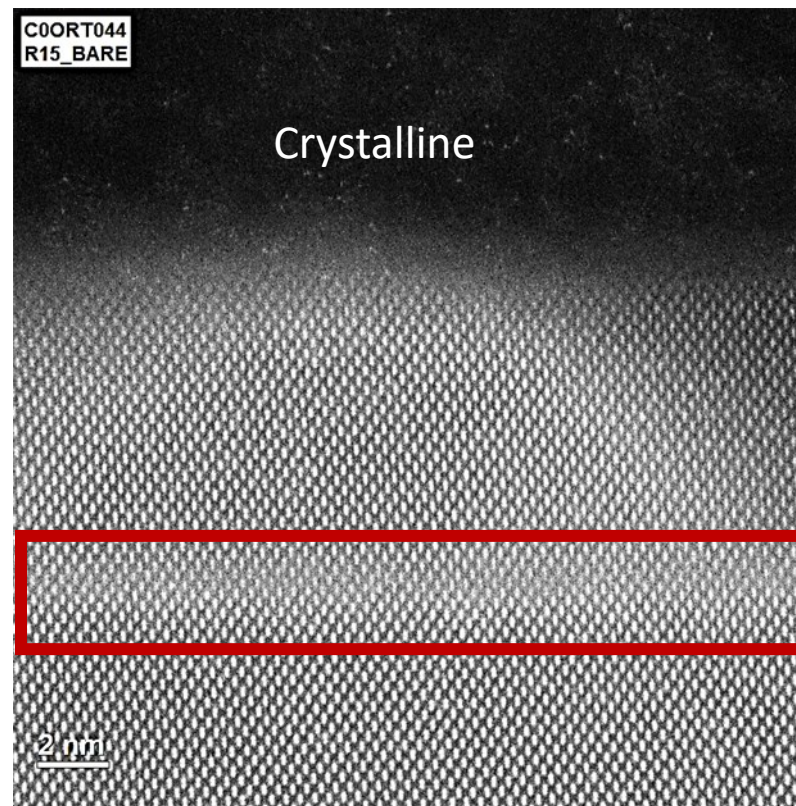
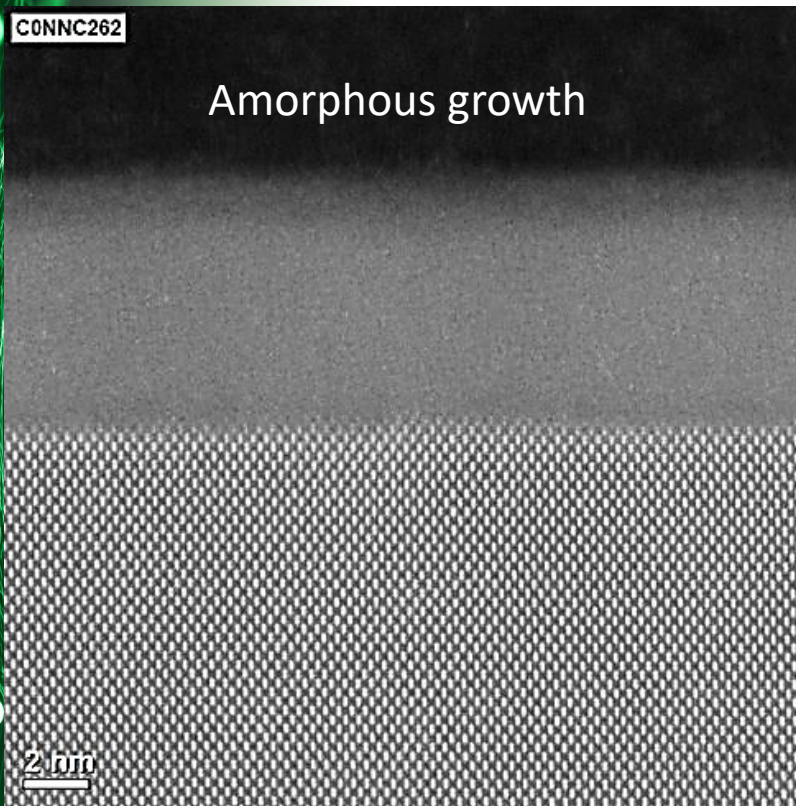
TEM (transmission electron microscopy) – crystallinity

- Crystallographic orientation of layer match substrate (001)
- Interface still blurry and visible islanding



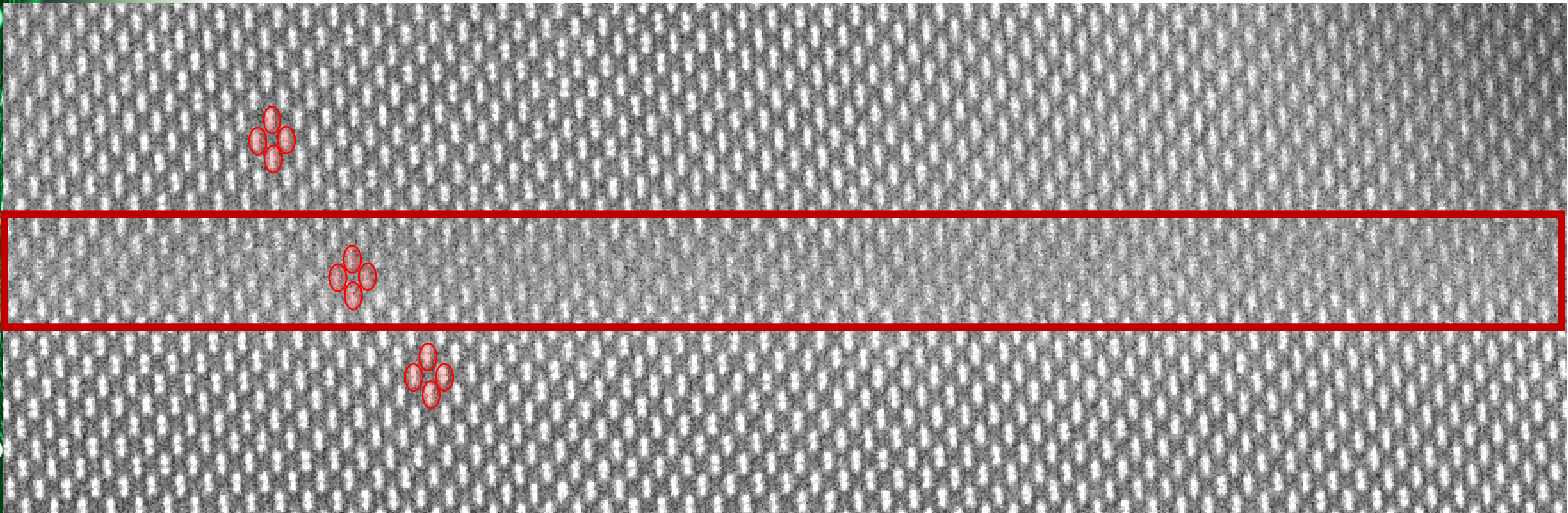
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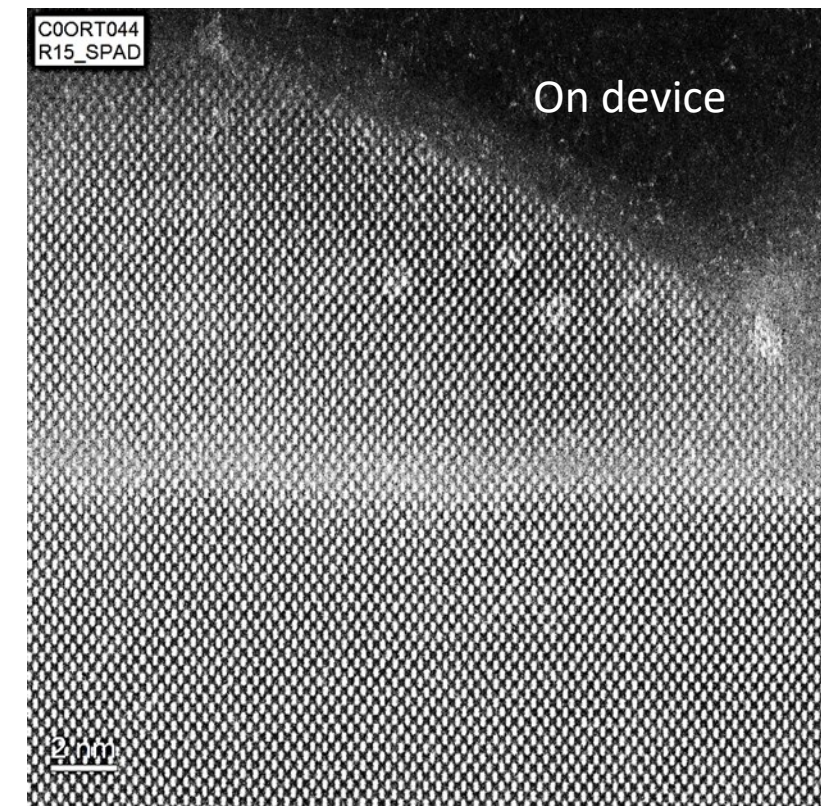
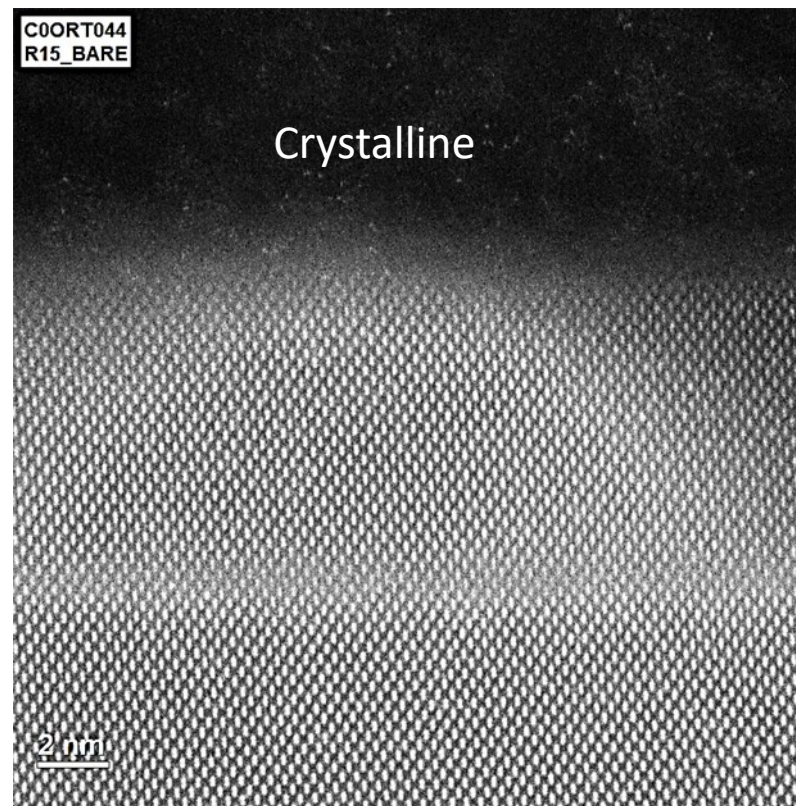
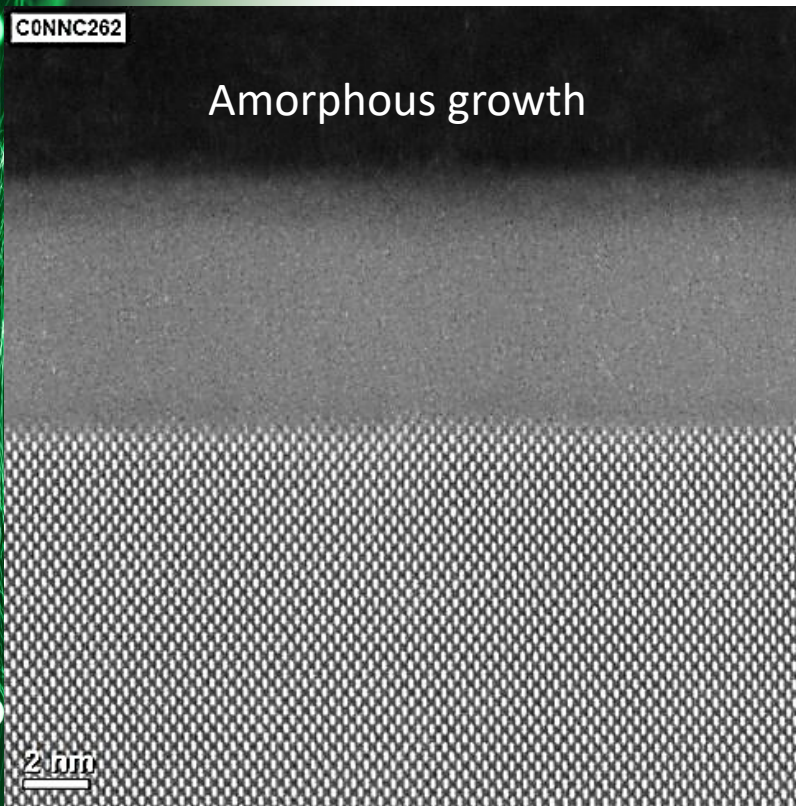
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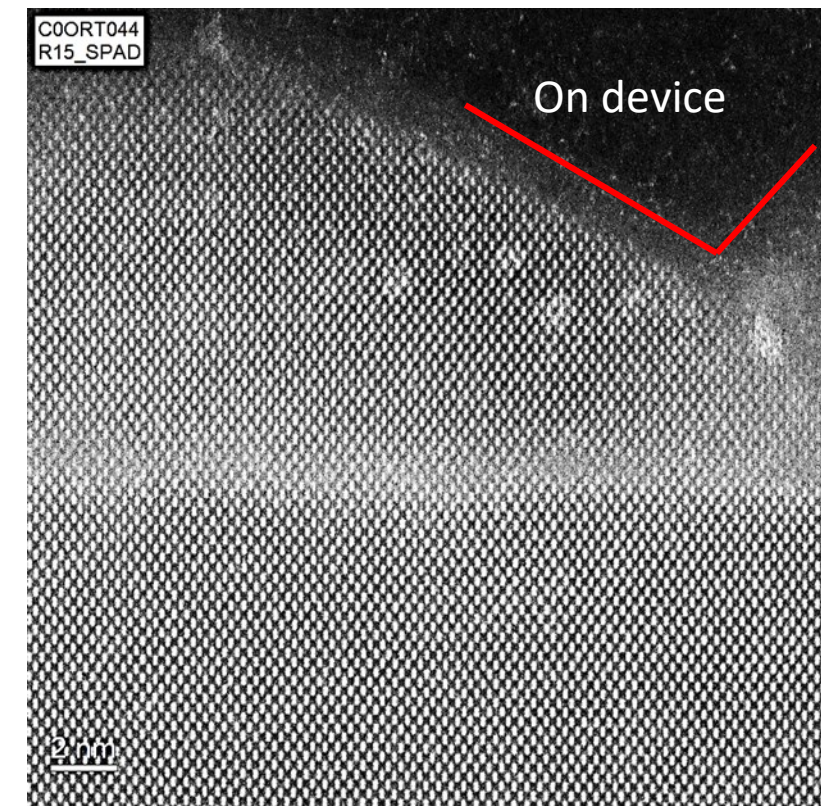
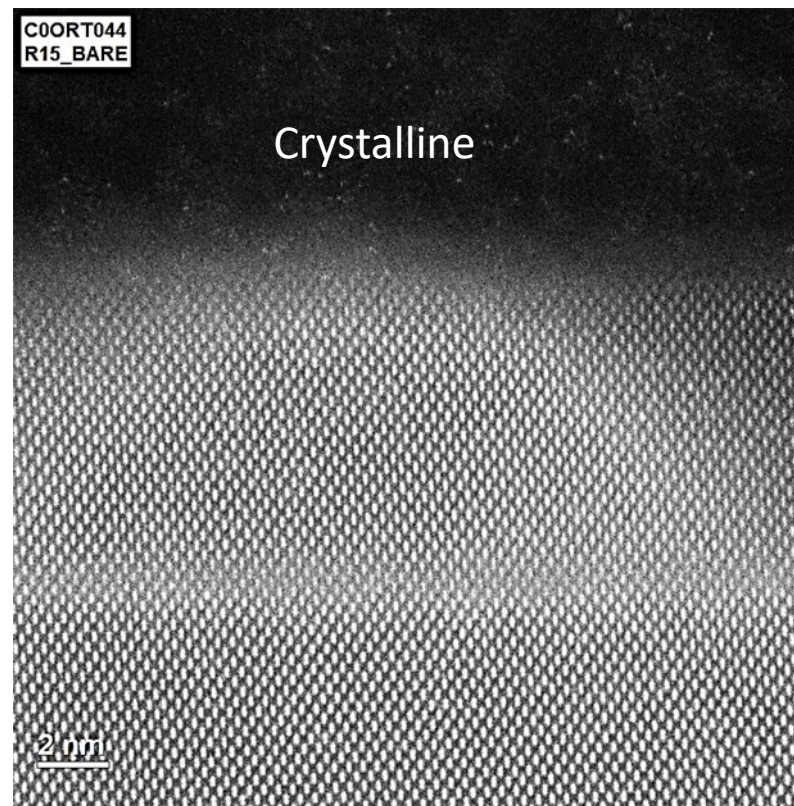
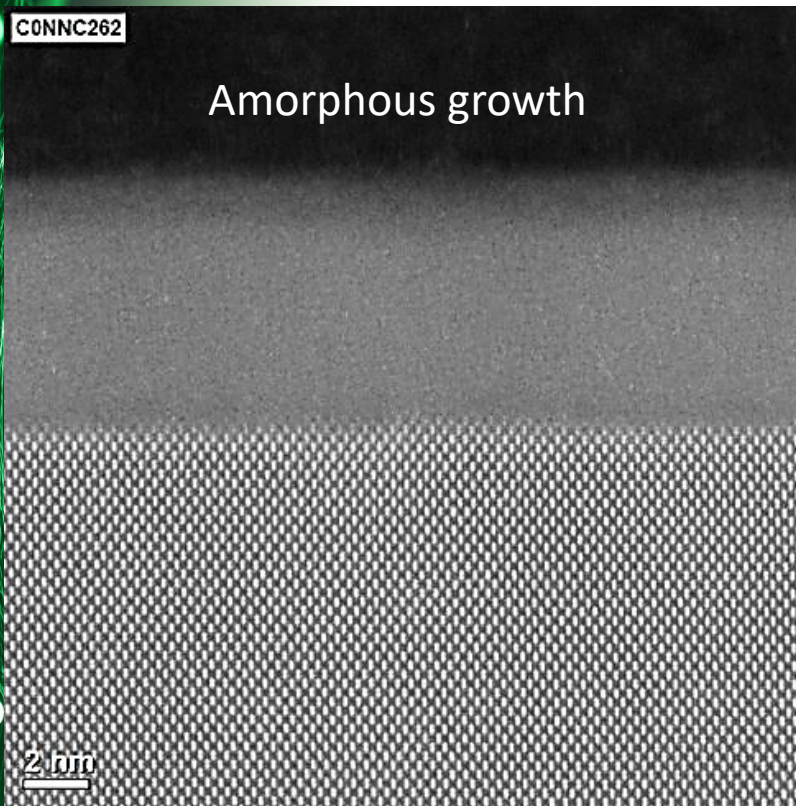
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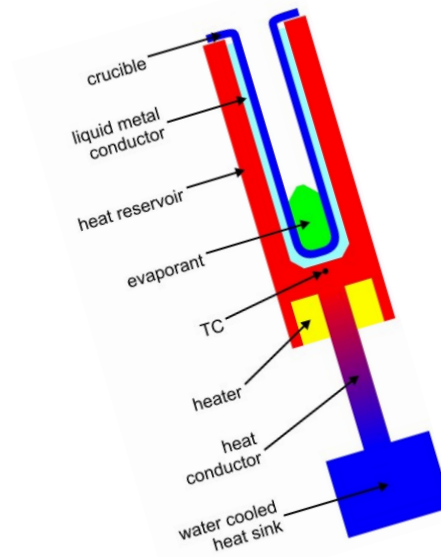
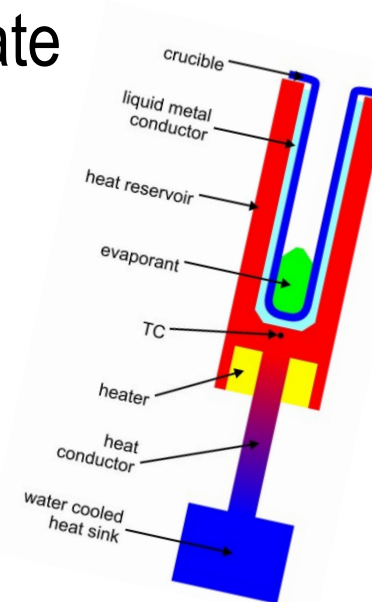
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Doping calibration

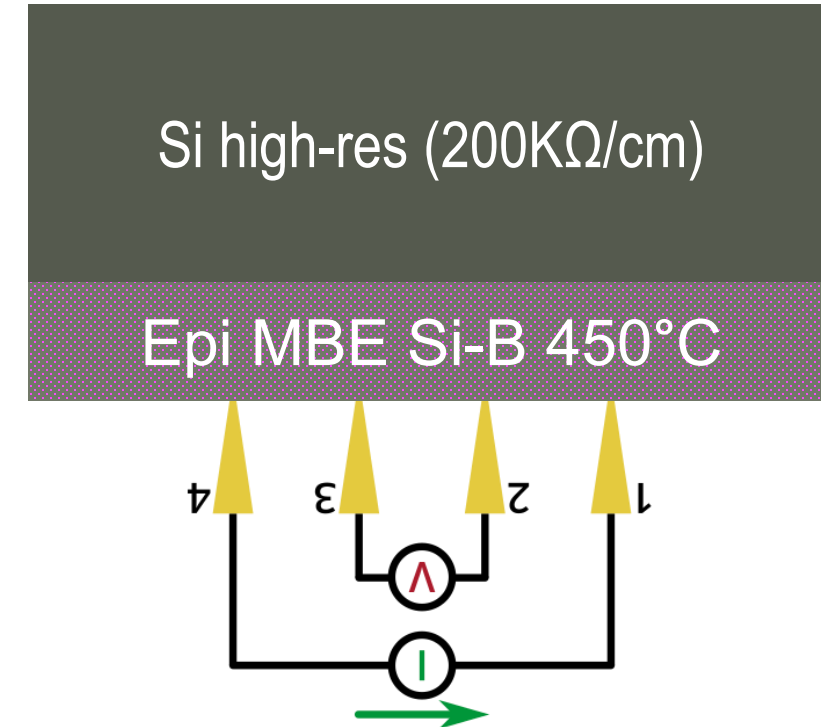
- Complex to characterize an $\sim 8\text{nm}$ layer (\$\$\$, precision..)
- Physical (atoms/cm^2) vs electronically active (useful) amount
- Co-deposition at fixed rates over high resistivity substrate at similar condition (cleaning, temperature)
- Electronically active boron from 4-points resistivity

Si high-res ($200\text{K}\Omega/\text{cm}$)

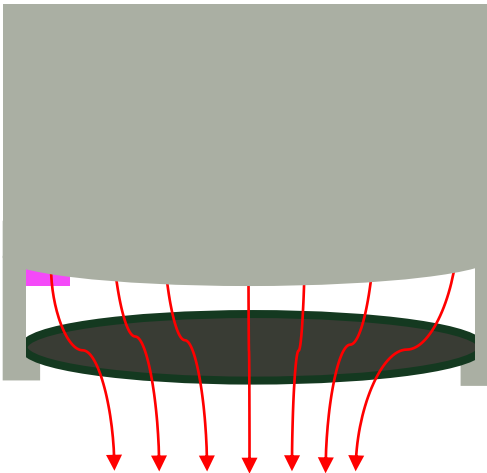
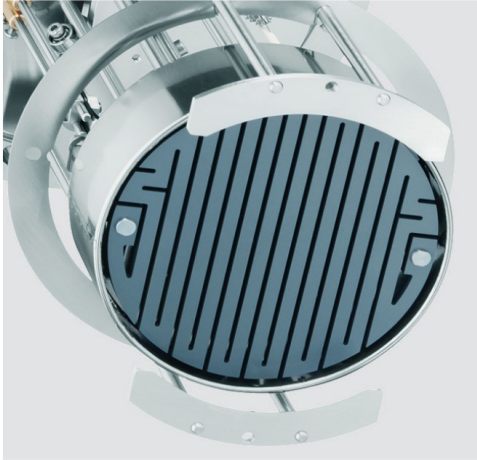


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Reproducibility – Thermal calibration

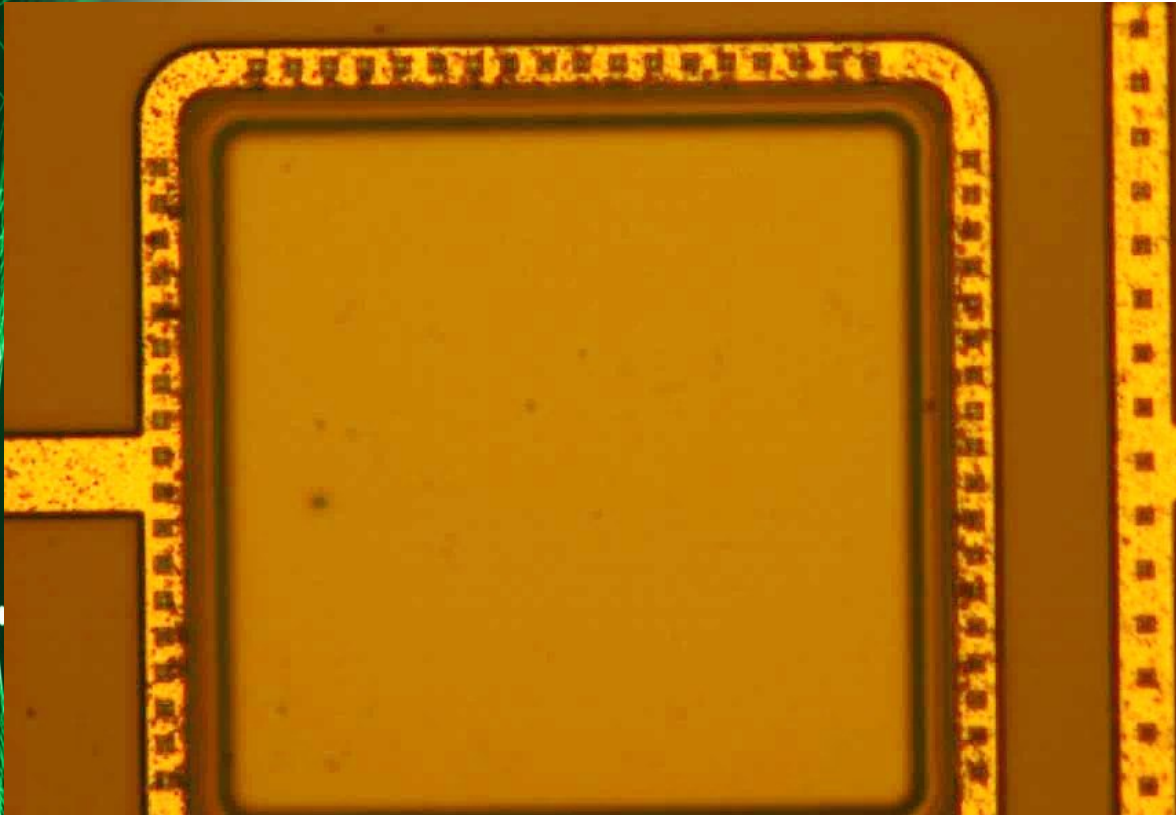


- Reproducibility study (crystalline quality) raised questions on process sturdiness (variation)
- Little overshoot (10-15°C) leads to irreversible damage
- Infrared heating onto “transparent” silicon, thermocouple inertia and molly holder

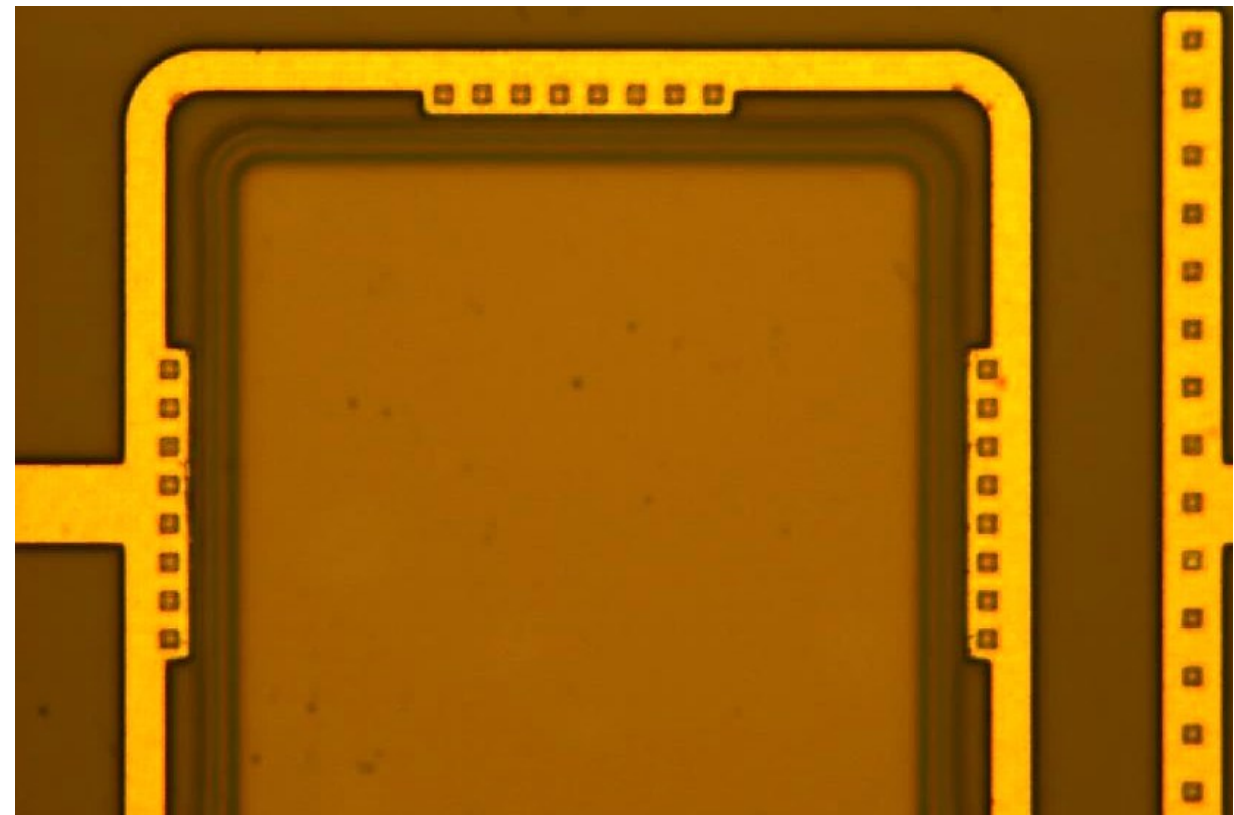
Thermal calibration



- Si
- p-type
- SiO₂
- ISDP
- n-type
- Metal



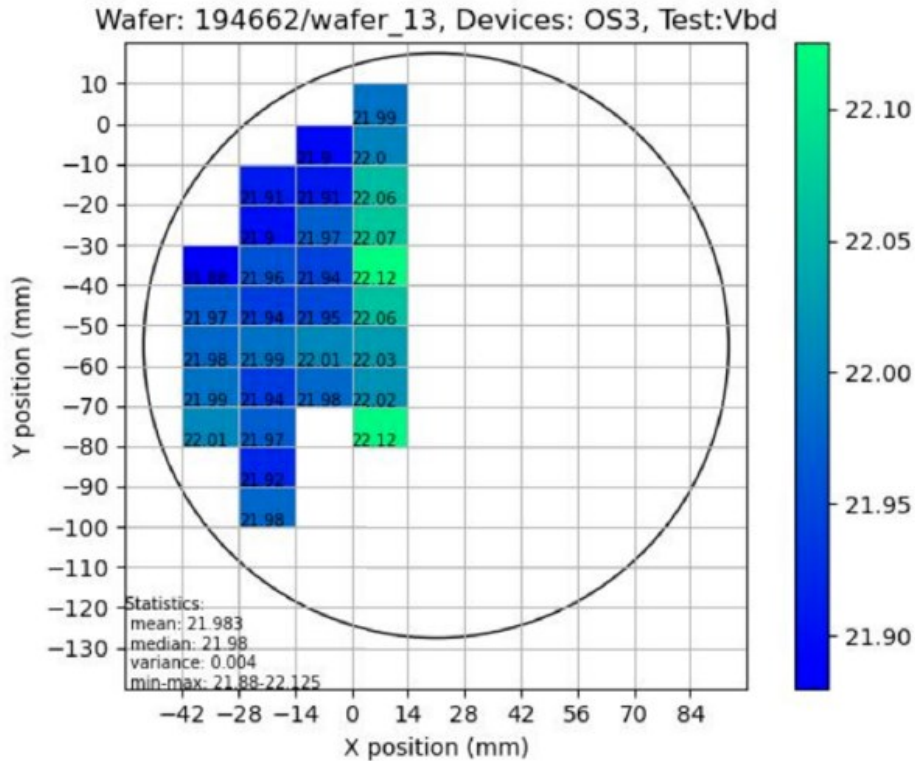
R15 ; PID rise used



GR3 ; Controlled % power rise

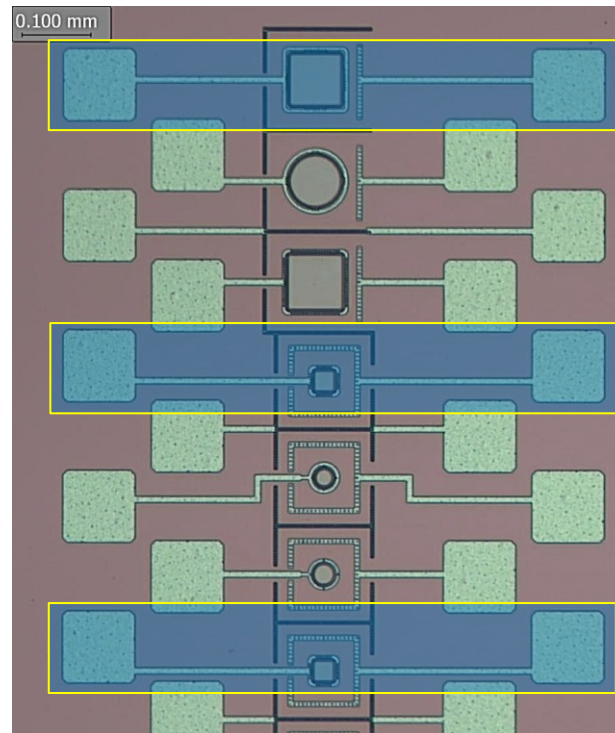
Electrical measurement – *device integrity (thermal effect)*

- Post-deposition **breakdown voltage** (V_{bd}) ~identical to unprocessed



Reference sample wafer Vdb mapping

F.Vachon, Masters thesis, Université de Sherbrooke, 2021.



Golden run (optimized) tested SPADs 1-4-7

Measurements overview

Reference data

Vbd (V) Average	Median (V)	STD dev (V)
21,983	21,98	0,063

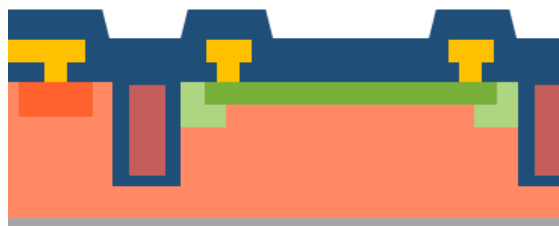
Processed sample data (24)

Vbd (V) Average	Median (V)	STD dev (V)
22,2	22,181	0,07

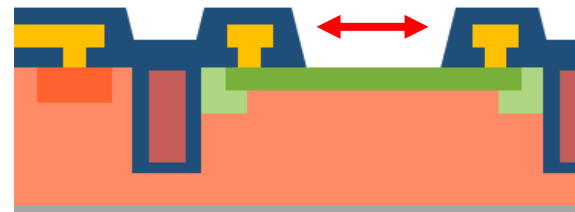
Photoelectrical measurements – *device integrity*

Dark count rate (measured amount of “photon” in the dark (noise))

- Oxide removal and chemical cleaning ups noise (x20)
- Redeposition passivates, still ups noise (chemical cleaning)



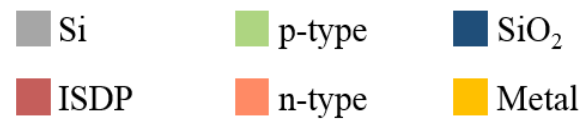
~5 kHz avg.



~100 kHz avg.



~9 kHz avg.

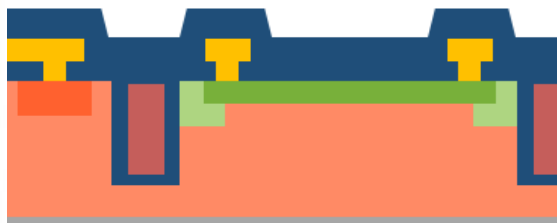


*all measurement are @R.T. on a repeated 36 μm² square SPAD

Photoelectrical measurements – *device integrity*

After pulsing (retriggering)

- Reduction on treated device ($\sim x2$)
- Overall low rates ($<5\%$)



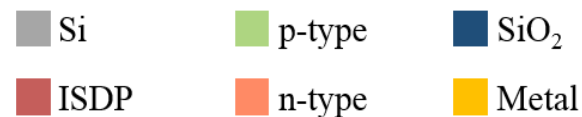
$\sim 5\%$ avg.



$\sim 3.88\%$ avg.*



$\sim 2\%$ avg.



*AP measurement on non-dep SPAD could be falsen by high DCR (10^6+)

Conclusion & future work

Complete parameter study and first functional (electric and photoelectric) tests for δ -doping on FSI SPADs have been done.

Incoming:

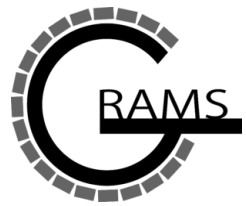
- Full VUV photoelectric tests (complete array, 175nm, cryo)
- Further optimization of the process (cleaning, recipe, growth)
- Scale-up to wafers (4")

Further down the road:

- Industrial (TDSI) adaptation

in order to make our solution available to the public.

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GRAMS

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- Bouraoui Ilahi
- Tadeas Hanus
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- Peter Margetak
- Austin de Ste Croix

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Fonds de recherche
sur la nature
et les technologies



Question?

Thanks for listening!

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Growth details

Pressures:

- Base: 3×10^{-11} torr
- Deposition: 1×10^{-9} torr

Pre-bake: by steps, 2h @200°C, 1h @350°C, then raised to growth temp (450°C)

Deposition: 16min @450°C

- E-Beam silicon source ~1nm/min
- Boron Knusden cell @1250°C ($\sim 10^{20}$ /cm²)