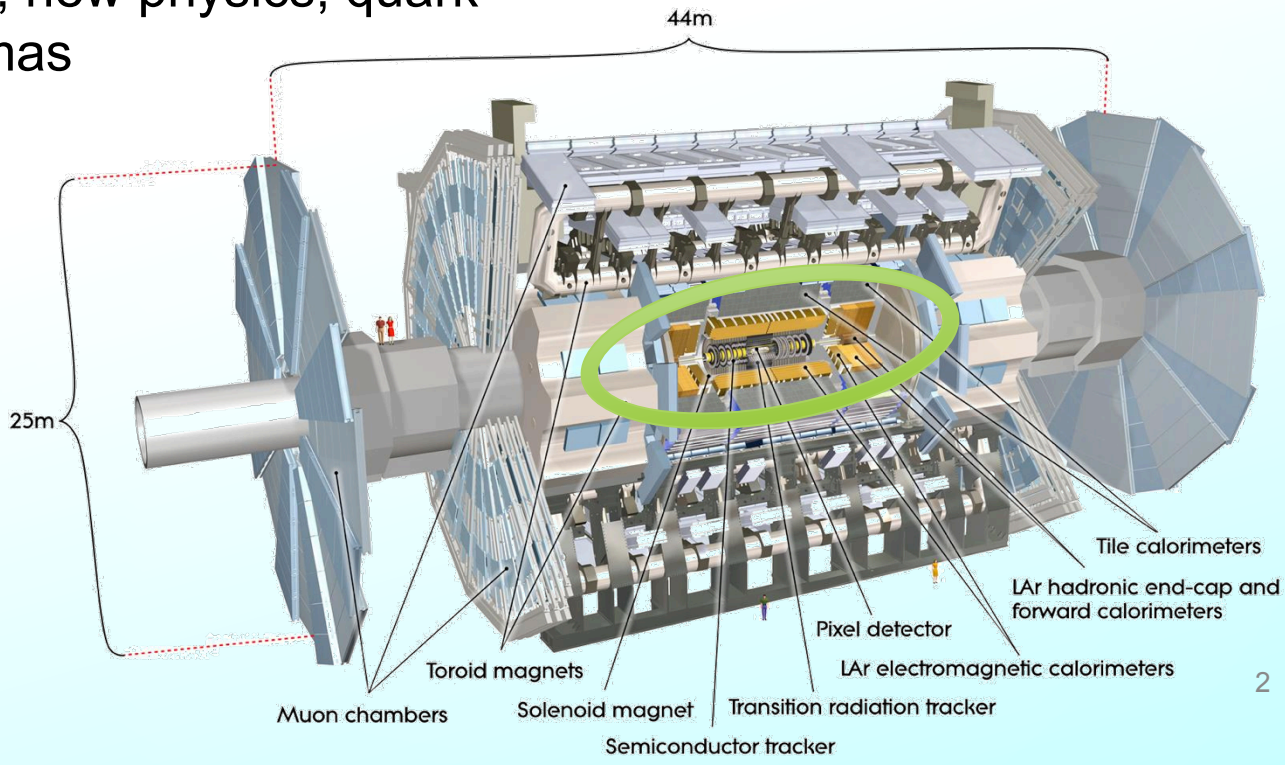
PROPOSED CMOS-BASED SENSORS FOR THE ATLAS DETECTOR: CHESS-2

Robin Newhouse
University of British Columbia

ATLAS DETECTOR

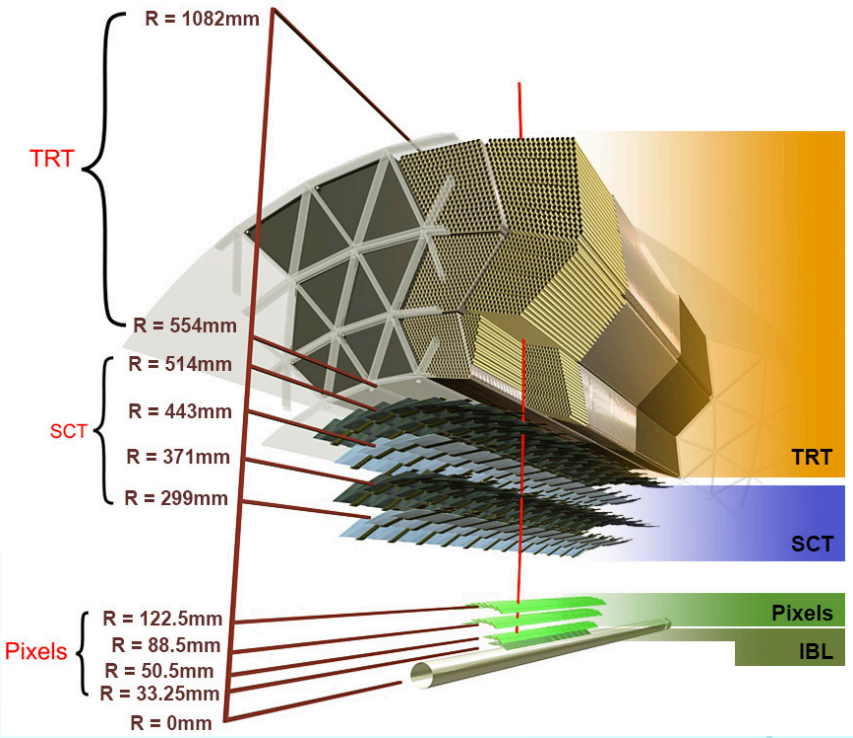
- Detects particles produced by **proton-proton collisions** in the Large Hadron Collider
- Studies: origin of mass, nature of dark matter, new physics, quark-gluon plasmas



https://inspirehep.net/

INNER DETECTOR STRUCTURE

- Inner detector measures charged particle **trajectory**
- Inner tracker radius: ~1 m
  - Pixels
  - Semiconductor Tracker
  - Transition Radiation Tracker



ATLAS Inner Tracker

ATL-PHYS-PUB-2015-018

WHAT'S NEXT FOR THE LHC?

$\sqrt{s}$ = 7-8 TeV $L=0.8\times10^{34}$ cm^{-2} s^{-1}

28 fb^{-1}

First shutdown

$\sqrt{s}$ = 13 TeV $L=1.4\times10^{34}$ cm^{-2} s^{-1}

36 fb^{-1}

~150 fb^{-1}

$\sqrt{s}$ = 13-14 TeV $L=1.5\text{-}1.7\times10^{34}$ cm^{-2} s^{-1}

Phase 1 upgrade

$\sqrt{s}$ = 14 TeV $L=2\times10^{34}$ cm^{-2} s^{-1}
Pileup: 20 – 40

~300 fb^{-1}

HL-LHC Phase 2 upgrade

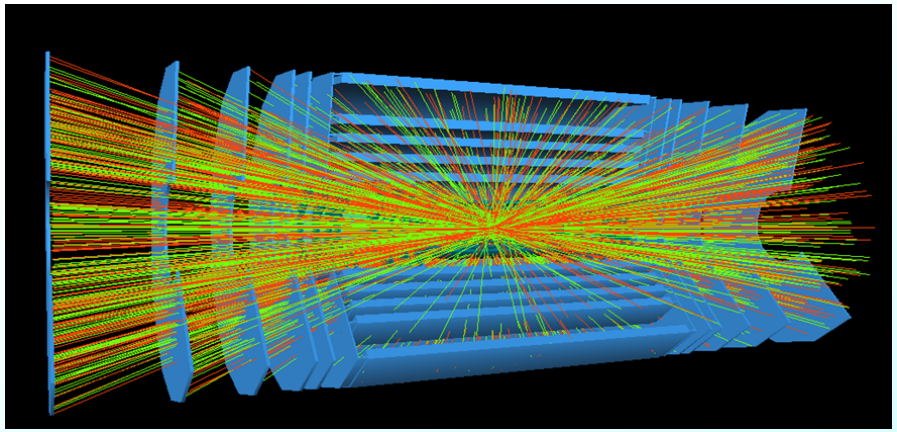
$\sqrt{s}$ = 14 TeV $L=5\times10^{34}$ cm^{-2} s^{-1}
Pileup: 140 – 200

~300 fb^{-1} / year

Slide Credit: Wojtek Fedorko

MOTIVATION TO REPLACE INNER DETECTOR

- Must handle significantly **increased luminosity**
- Issues
  - Bandwidth saturation
  - Detector occupancy
  - Radiation damage
- Requires a **complete replacement**

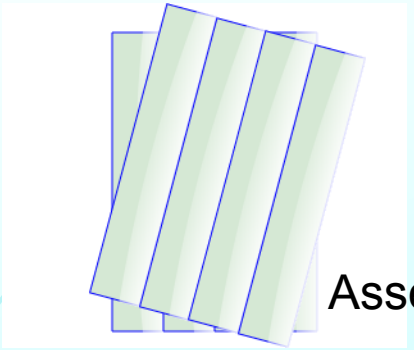


Pileup in the inner detector

ATLAS Upgrade for the HL-LHC: Meeting the challenges of a five-fold increase in collision rate - Vankov, Peter
EPJ Web Conf. 28 (2012) 12069 arXiv:1201.5469 [physics.ins-det] ATL-UPGRADE-PROC-2012-003

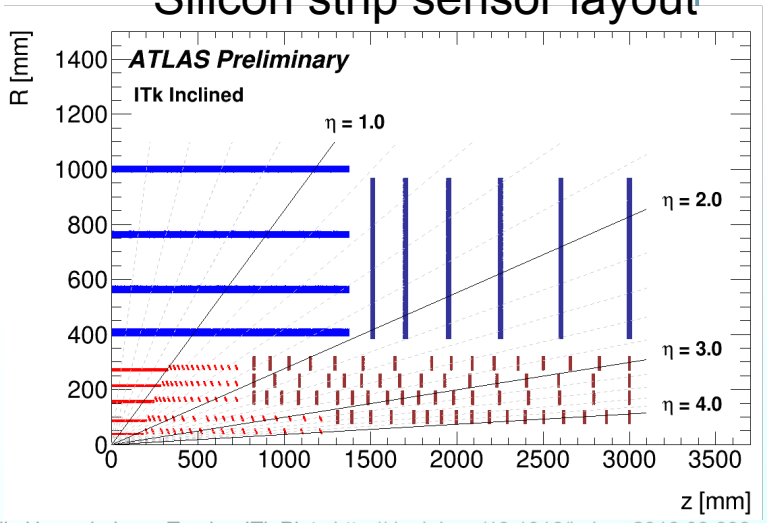
BASELINE TECHNOLOGY

- Plan to replace the inner detector with a new **all-silicon detector**
- **Two detectors**
  - **Pixel** detector: **39-271 mm** radius
  - Silicon **strip** detector: **405-1000 mm** radius
- Silicon strips: **over 200 m² silicon!**

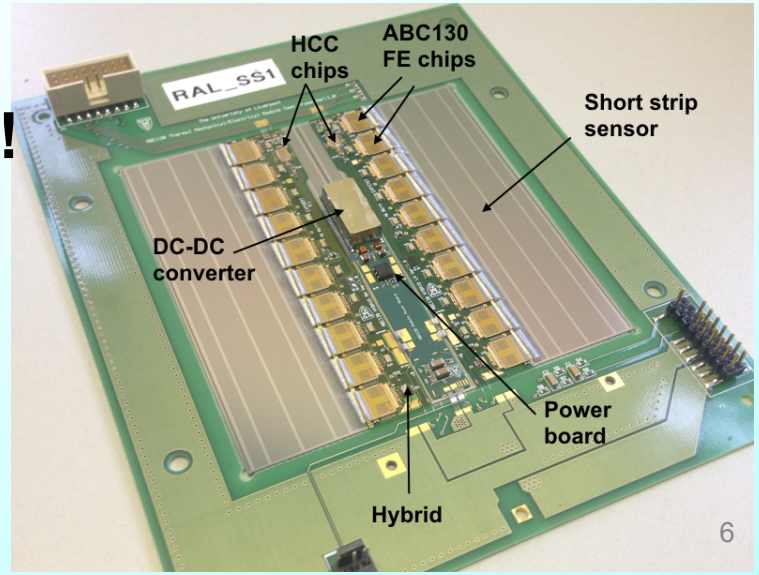


Assembled silicon strip sensor

Silicon strip sensor layout

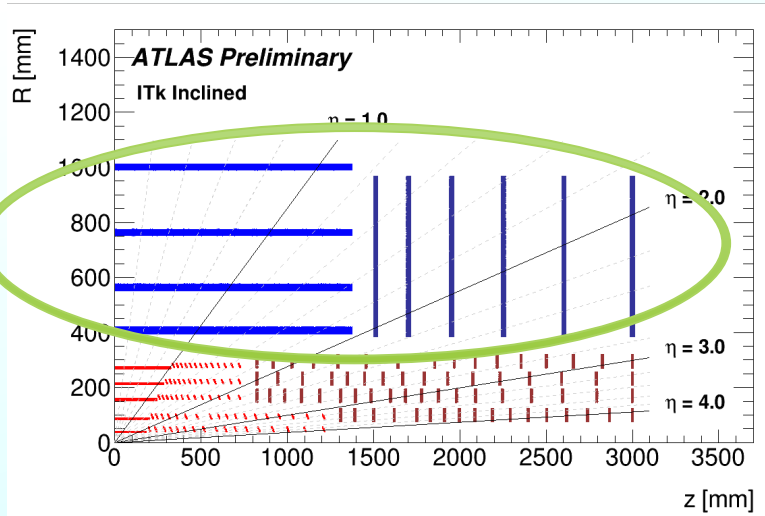


Public Upgrade Inner Tracker ITk Plots http://dx.doi.org/10.1016/j.nima.2016.03.099



ALTERNATIVE: HIGH-VOLTAGE CMOS DETECTORS

- Alternative proposed sensor technology
- Potential advantages over strip sensors
  - Reduced material budget
  - Assembly time/complexity
  - Commercial fabrication
  - Reduced cost
  - Spatial resolution



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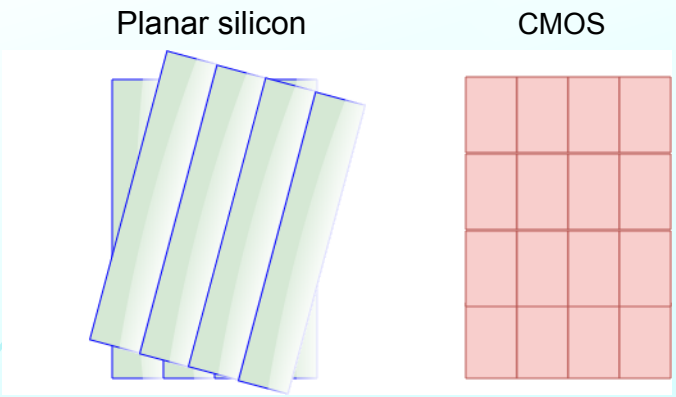


CMOS: FUNDAMENTAL DIFFERENCES

- "**Monolithic**" chip: Readout electronics are **integrated** with the sensor
- Information exchange to readout chips uses **fast digital bus**
  - Far fewer wire bonds than traditional one bond per channel
- Inherently **pixel-like** sensor
  - Row+column readout gives longitudinal information
  - Could reduce silicon area by ~1/2

STATUS

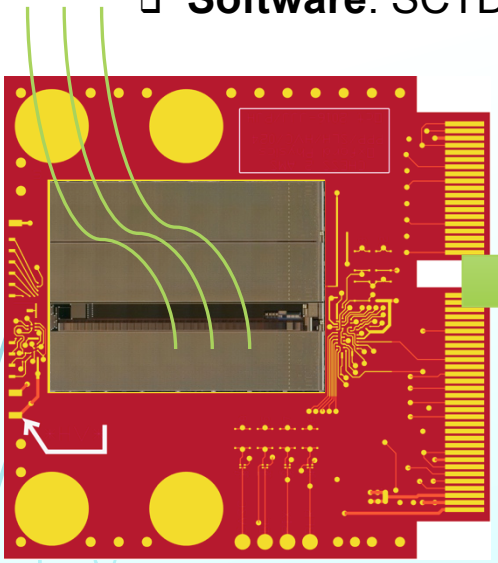
- CHESS-1
  - Pixel response
  - Can the pixels handle **radiation**?
    - Answer: so far, **yes**
  - Fadayev et al. characterize HVCMOS after irradiation by **neutrons** and **protons**
    - http://dx.doi.org/10.1016/j.nima.2016.05.092
  - Mandić et al. with **neutrons**
    - https://arxiv.org/abs/1701.05033

- CHESS-2
  - System Response
  - Can we build a **full prototype**?
  - Match the planned **readout protocol** and **physical architecture**
  - In progress

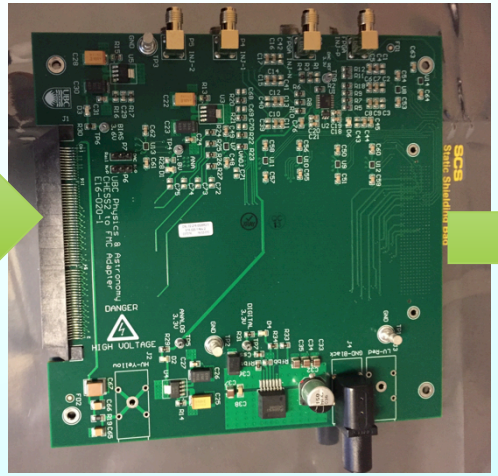
OUR CURRENT WORK
READOUT HARDWARE AND SOFTWARE

- Full test system will include:
  - CHESS-2 **digital daughterboard** designed at SLAC.
  - CHESS-2 to **FMC adaptor board** designed at UBC.
    - Supplies power, bias voltage, FMC communication to FPGA
  - Data acquisition **(DAQ) board**: Digilent's Nexys Video FPGA
  - **Firmware**: ITSDAQ (ITk Strips Data acquisition)
  - **Software**: SCTDAQ (SemiConductor Tracker Data acquisition)

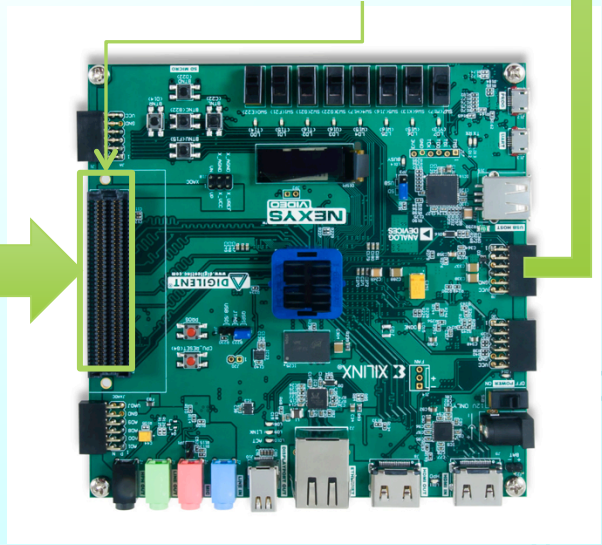
FMC
FPGA Mezzanine Card



Digital Daughterboard



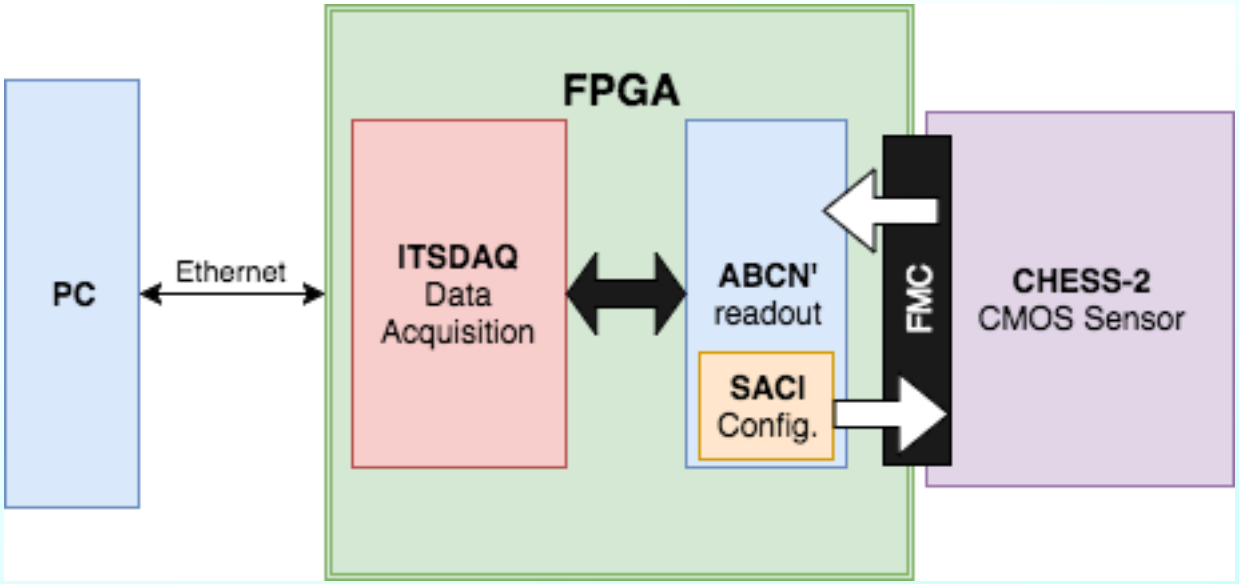
Adaptor board



Nexys Video FPGA

MY ROLE
READOUT SOFTWARE AND FIRMWARE

- Develop robust communication package for **configuration and data readout**
- Developing firmware to communicate with the ASIC control
- Use existing **SACI communication** protocol to define packet contents



NEXT STEPS

- Completion and testing of **readout software**
- **Integration** into the current mechanical and electrical system (a full module)
- Examination of signal response with **charge injection** on CHESS sensor (simulating signals)
- Single chip **ASIC** to replace FPGA prototype

SUMMARY

- ATLAS inner tracker will be replaced to **cope with high-radiation** environment of High-Luminosity LHC program
- High Voltage **CMOS sensors** are proposed as an alternative to the baseline silicon strip sensors
- CHESS-2 program will construct a **fully integrated prototype** for testing and proof-of-concept
- Readout software and firmware being constructed as to be **compatible with planned ITk readout infrastructure**

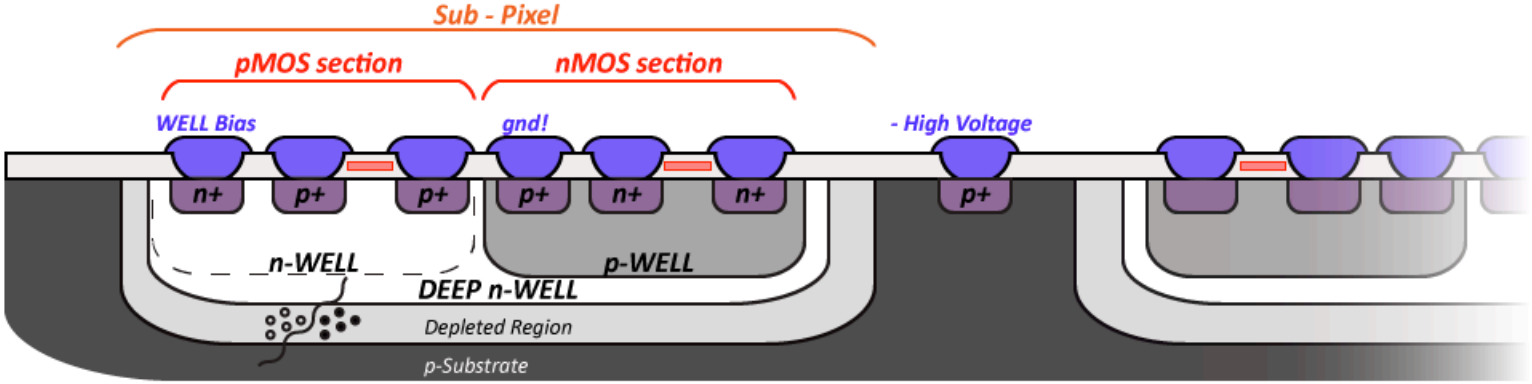
QUESTIONS?

BACKUP SLIDES

CHESS-2 CROSS SECTION

- CHESS-2: “CMOS HV/HR Evaluation for Strip Sensors”
- **Electron-hole pairs** (caused by ionizing particles) separated and quickly collected by drift
- A lightly doped deep n-well (DNW) in p-type substrate is used as charge collecting electrode
- The p-n junction is partially depleted by applying a reversed bias voltage

http://iopscience.iop.org/article/10.1088/1748-0221/10/03/C03033

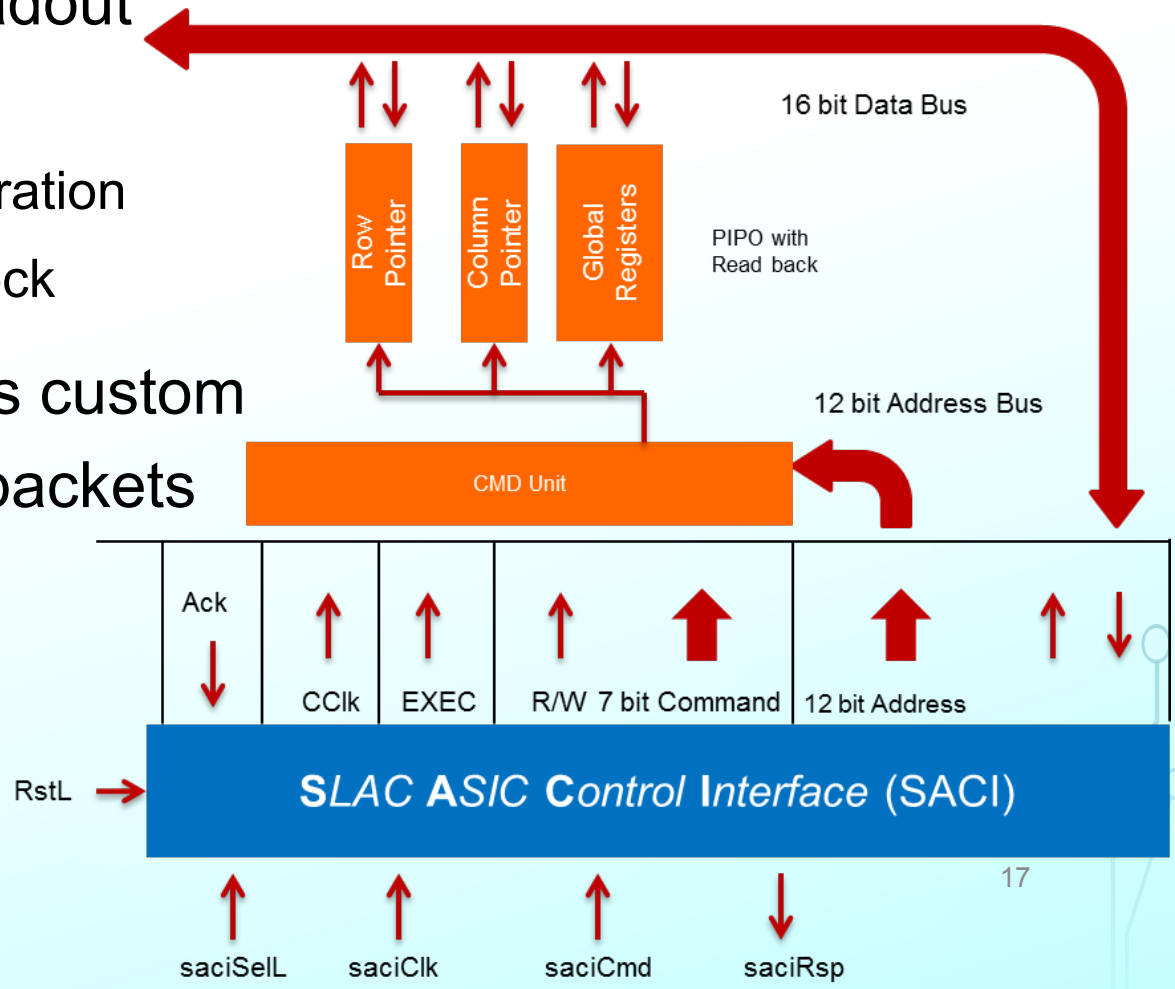


AMS 0.35µm HV Sensor and read-out on the same substrate.

P. Caragiulo *CHESS-2 AMS Design* http://www.slac.stanford.edu/exp/atlas/upgrade/

SACI COMMAND STRUCTURE (SLAC ASIC CONTROL INTERFACE)

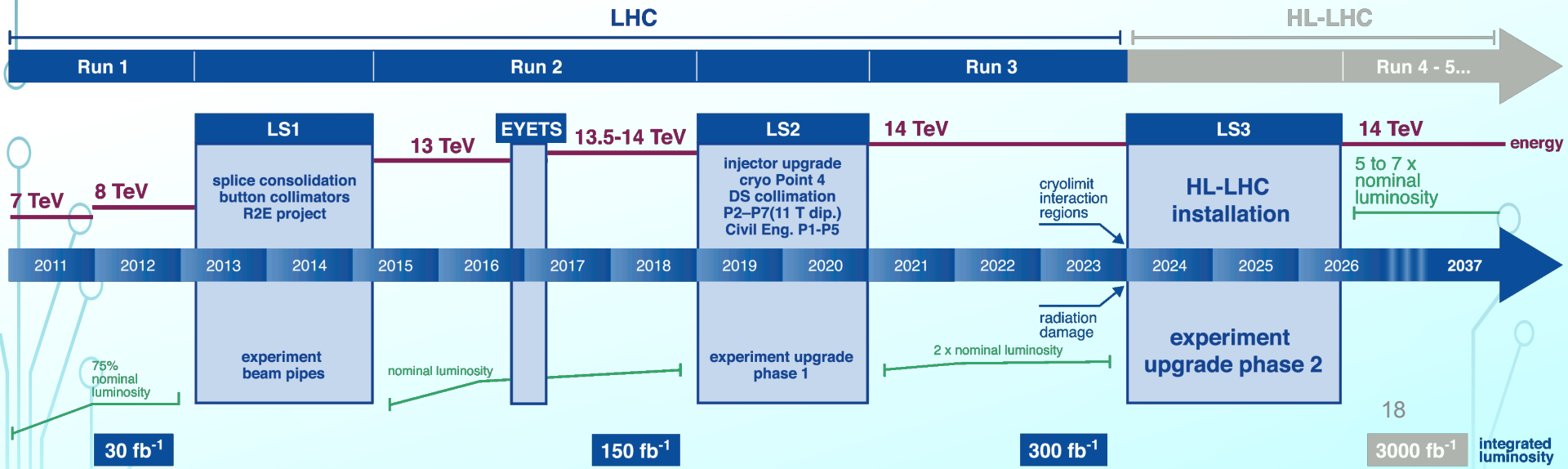
- SACI configures readout electronics
  - Pixel matrix configuration
  - Initialize 40MHz Clock
- Instructions come as custom serialized ethernet packets



NEXT STEPS FOR ATLAS

- High-Luminosity LHC upgrades will increase the dataset

Year: Run	CoM Energy (TeV)	Integrated Luminosity (fb^{-1})	Instantaneous Luminosity ($cm^{-2}s^{-1}$)
2010: Run 1	7	~30	$8x10^{33}$ (2012)
2017: Run 2	13	~150	$1.37x10^{34}$ (2016)
2020: Run 3	14	~300	$2x10^{34}$
2025: HL-LHC	14	~3000	$5\text{-}7x10^{34}$



http://hilumilhc.web.cern.ch/about/hl-lhc-project

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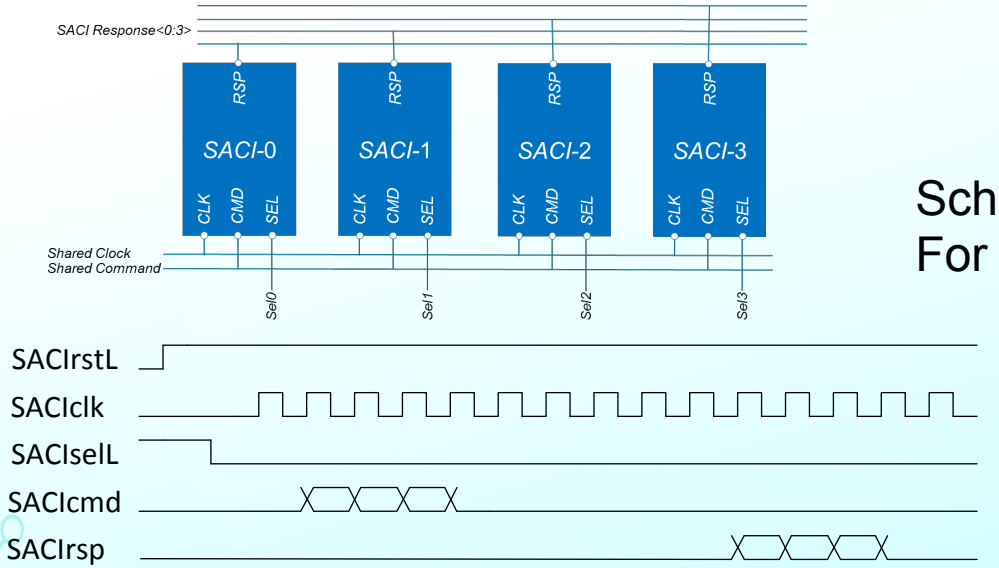
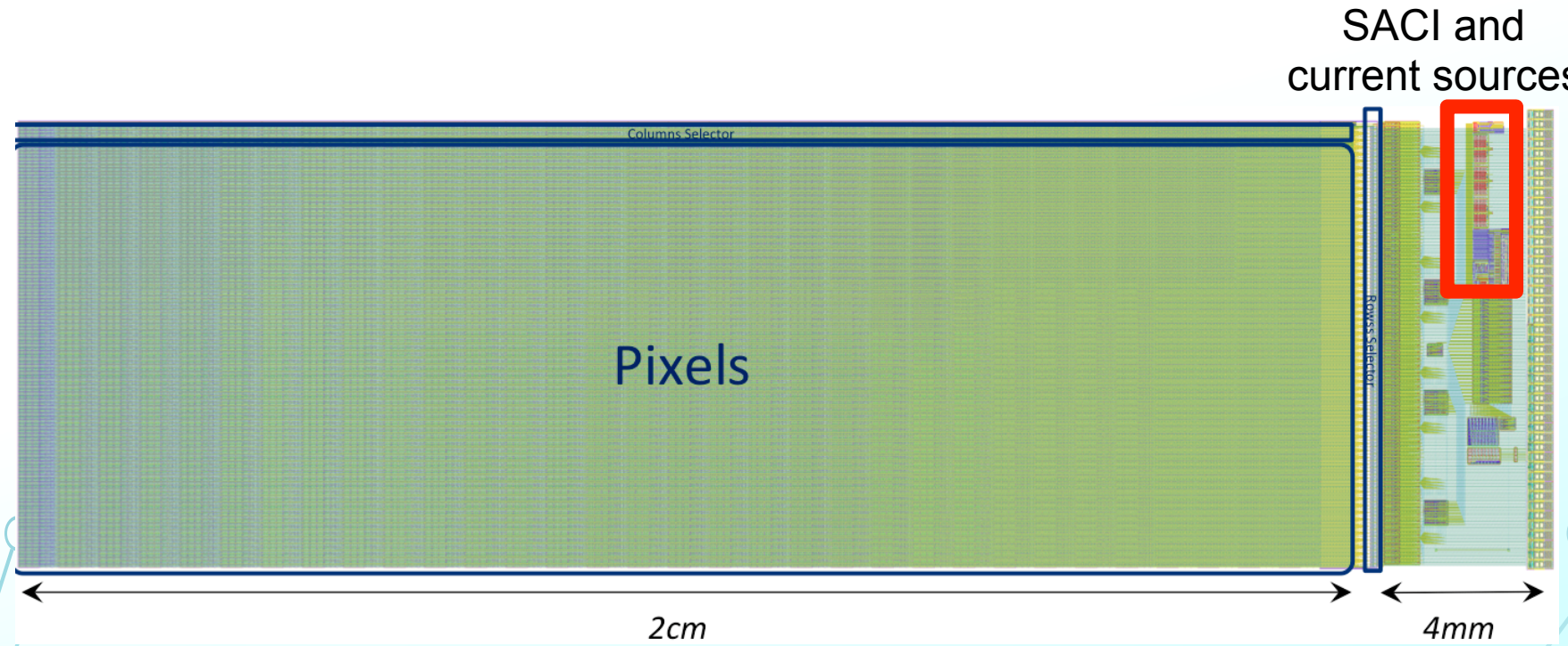


Schematic and example signals
For SACI configuration commands

CHESS-2 PHYSICAL STRUCTURE



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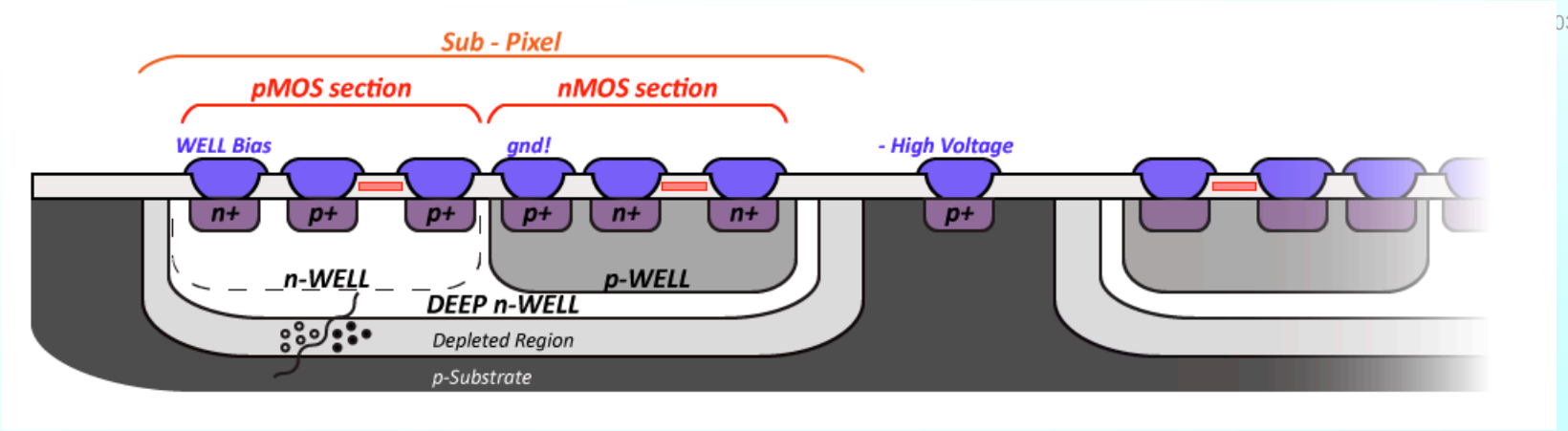

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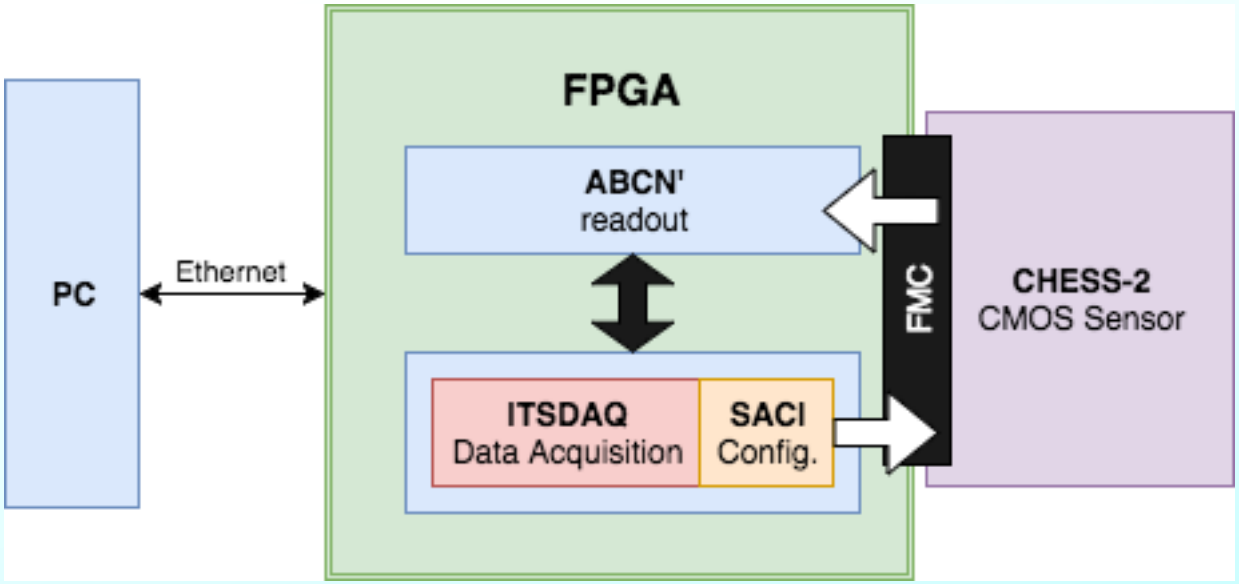
Phase 1



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