

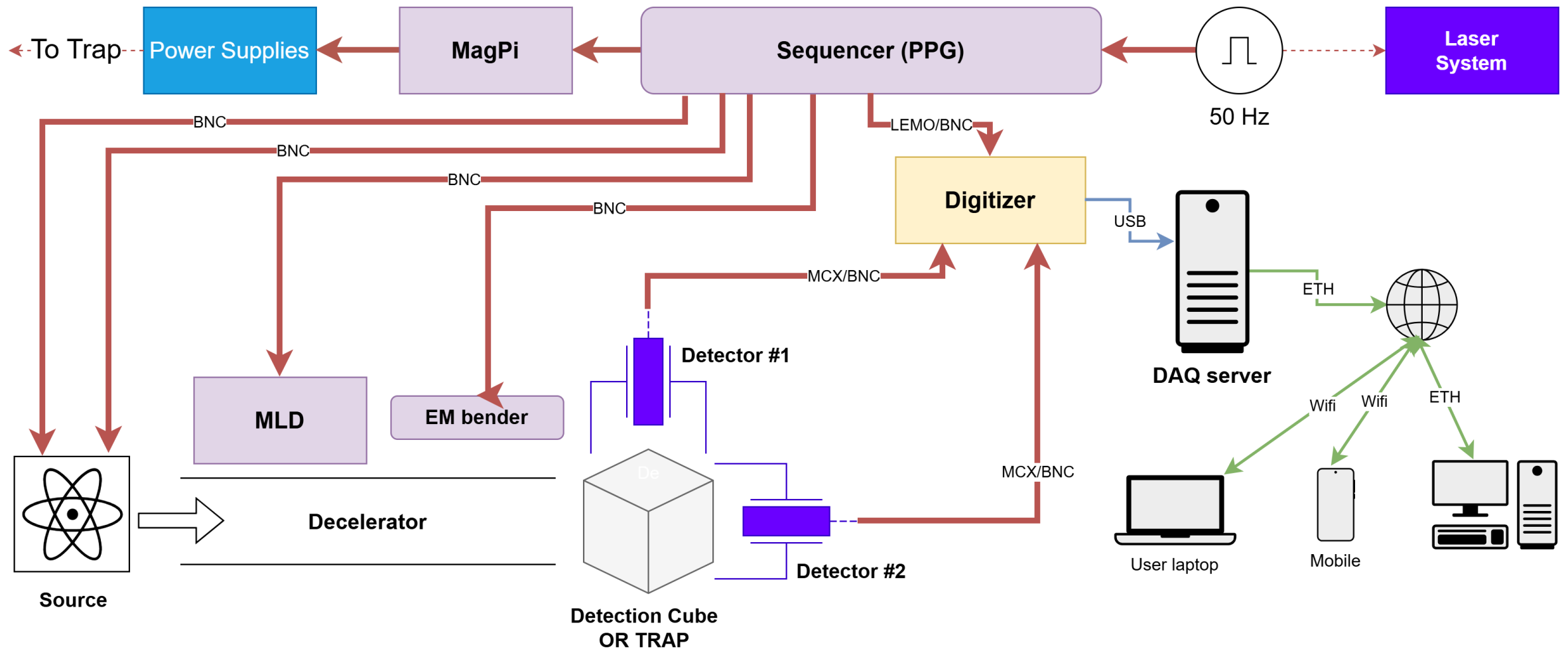
CS & Detectors update

Andrea + Lars + Zach + Kalib



Control System

- PPG → Sequencer → Control experiment's equipment by programmable digital I/O
- MagPi → Trap's magnets → Ramp the magnets to desired current via DAC

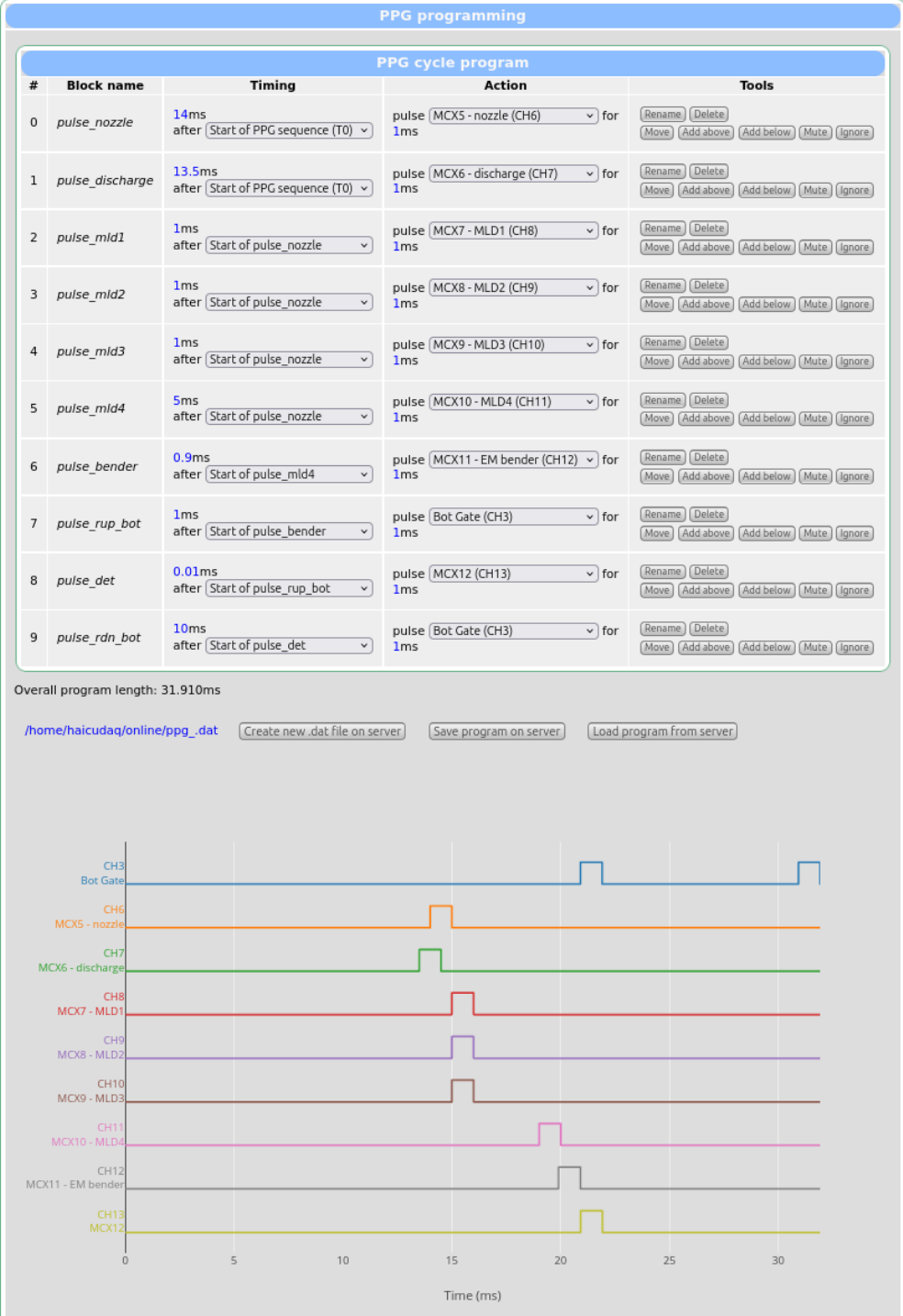


PPG capabilities (Lars)

- FPGA based **P**rogrammable **P**ulse **G**enerator
- 100MHz clock, i.e. 10ns resolution
- Up to 32 independent outputs
- Up to 16 gate inputs and 16 veto inputs
- External trigger input
- Inputs and outputs can be freely mapped to ribbon connectors on back panel or coax connectors on front panel
- Design modified from <https://daq00.triumf.ca/DaqWiki/index.php/VME-PPG32>

PPG User Interface (Lars)

- Sequences saved and loaded as hard-to read text file
- But convenient compiler with web-interface exists



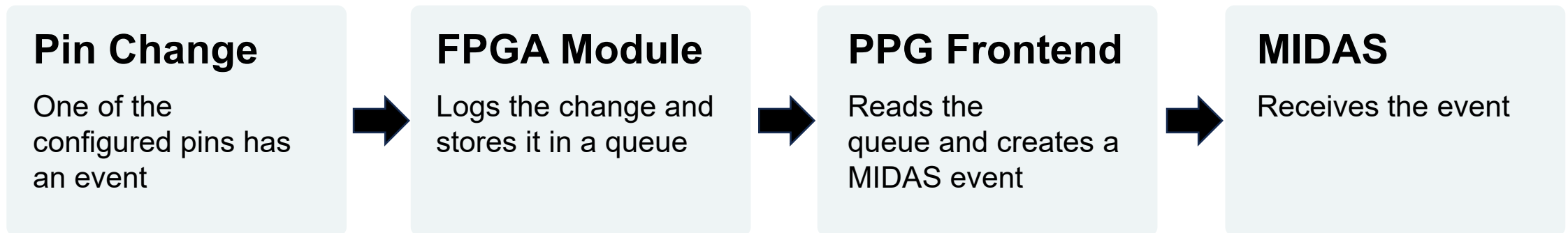
PPG firmware and software update (Kalib)

Goal

- Redeploy timestamping feature (as used in ALPHA)
- PPG sends timestamped pin changes to MIDAS.

Expected Result

- Changes on any configured pins are logged in MIDAS
- Each log contains the edge type, channel number, and a timestamp
- Pin names, edge configuration, and other useful settings are available in the ODB



Testing & Results (Kalib)

Receiving Data

Checked the new data pathways worked by modifying test_cb.exe which was made to read the old Chronobox logs. The FIFO status register and data output were both verified to work properly.

Decoding

Started with decoding FPGA output and printing to terminal. Using a function generator and oscilloscope, each pin was triggered and the log was checked and matched the expected output.

Sending Events

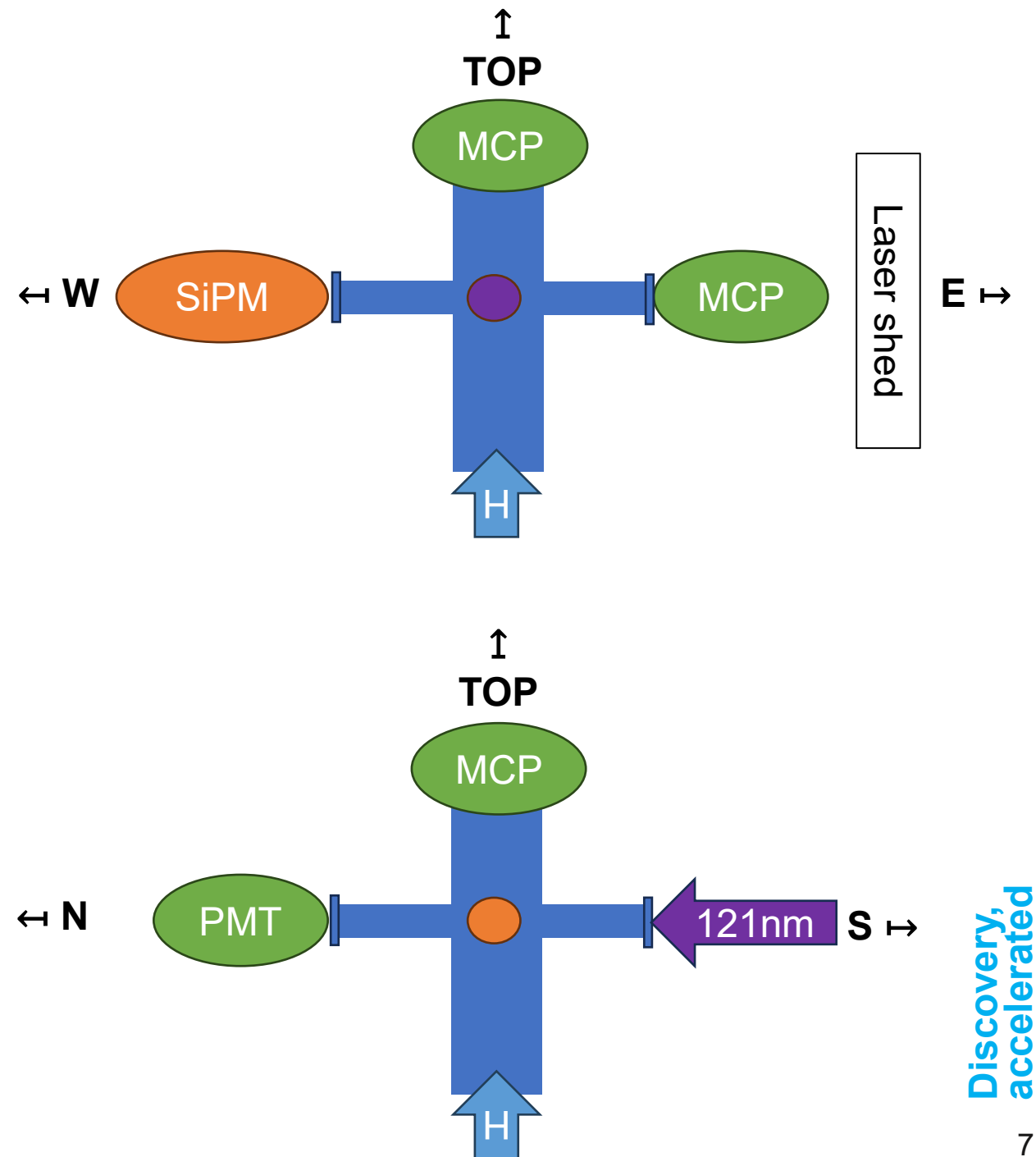
Sent data to MIDAS and decoded manually to compare to terminal outputs. Made sure no events were missed.

ODB Settings

Checked toggles enabled and disabled appropriate settings, added pin naming and matched to physical hardware. Checked events would not be sent while below the minimum event size selected.

Detectors Overview

- 4 SiPM Hamamatsu VUV4
- $\frac{1}{4}$ SiPM damaged, looking for replacement
- $\frac{3}{4}$ SiPM performance measured match literature (Zach)
- SiPM cooling maintains temperature within 0.1°
- MCP side – no update
- MCP front – ion detection option



SiPM in HAICU (Zach)

Breakdown Voltage:

Measured values (chans 0, 1, 3):

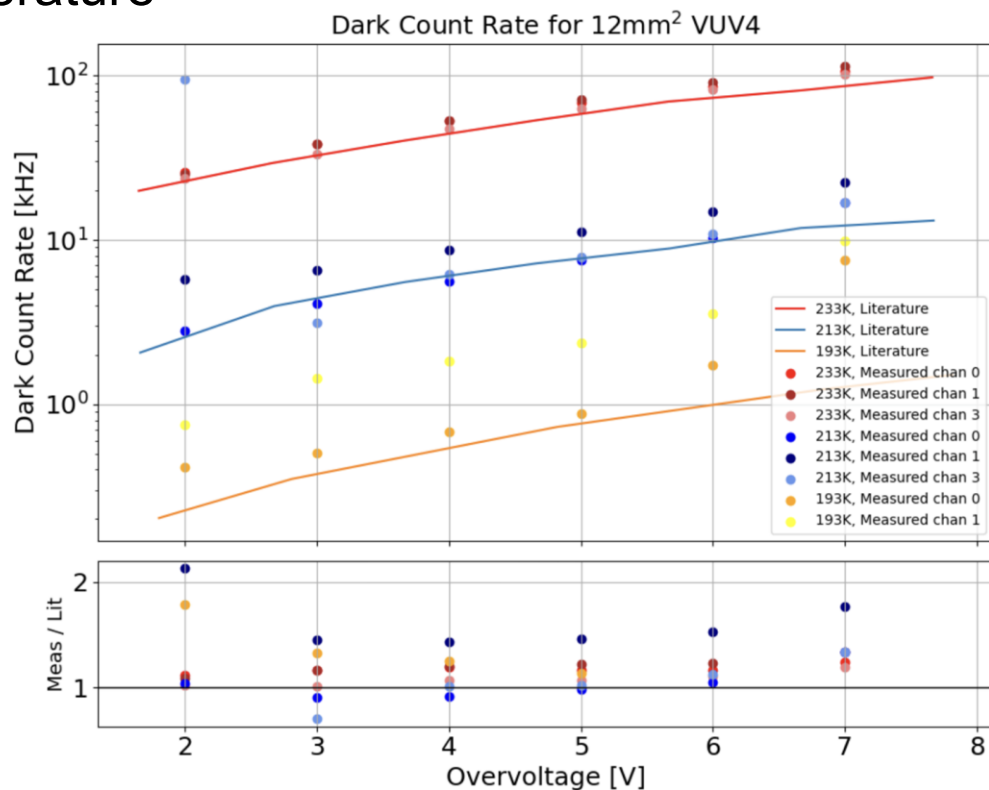
52.1 +/- 0.3 mV/K, 50.2 +/- 0.2 mV/K, 52.7 +/- 0.3 mV/K

Literature value: 50 ± 2 mV/K

(<https://arxiv.org/pdf/1903.03663>)

Dark Count Rate:

The measured DCR values were on average 30% higher than literature

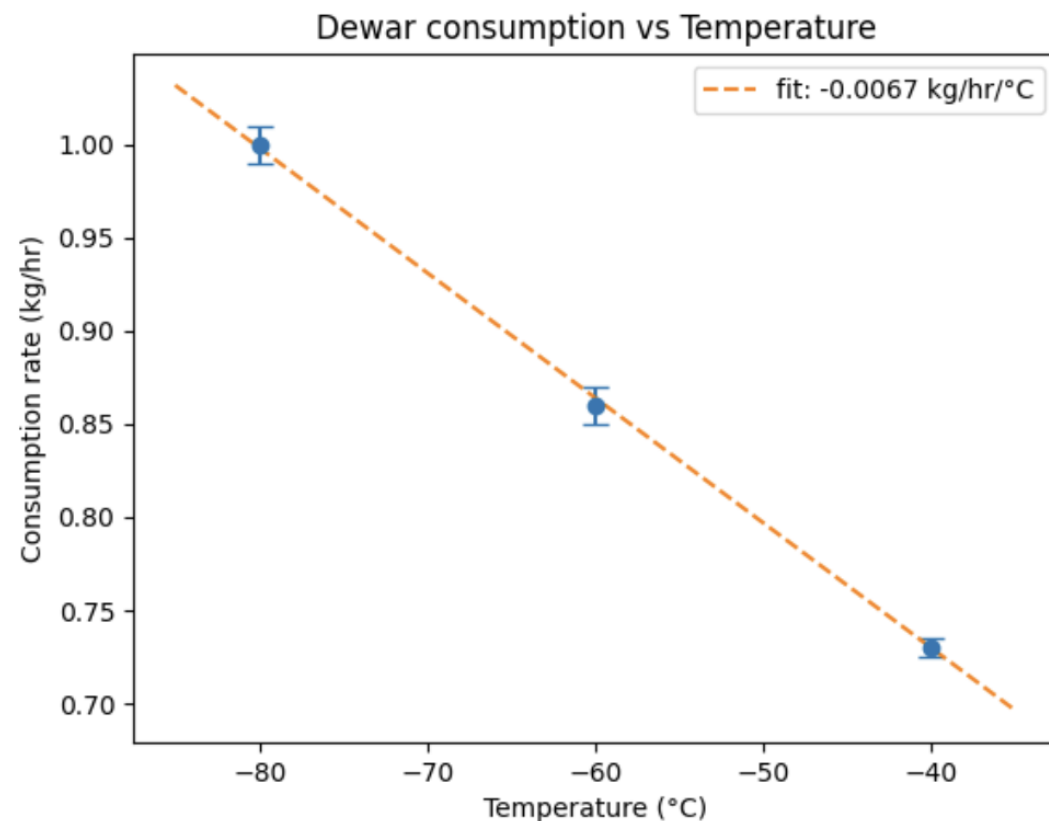


LN2 cryo cooling:

Holds temp within 0.1C of the set point
(RMS 0.046C)

Reached temperatures as low as -180C
(can likely go lower to the LN2 boiling point
-196C)

Dewar can be refilled while holding a steady
temperature

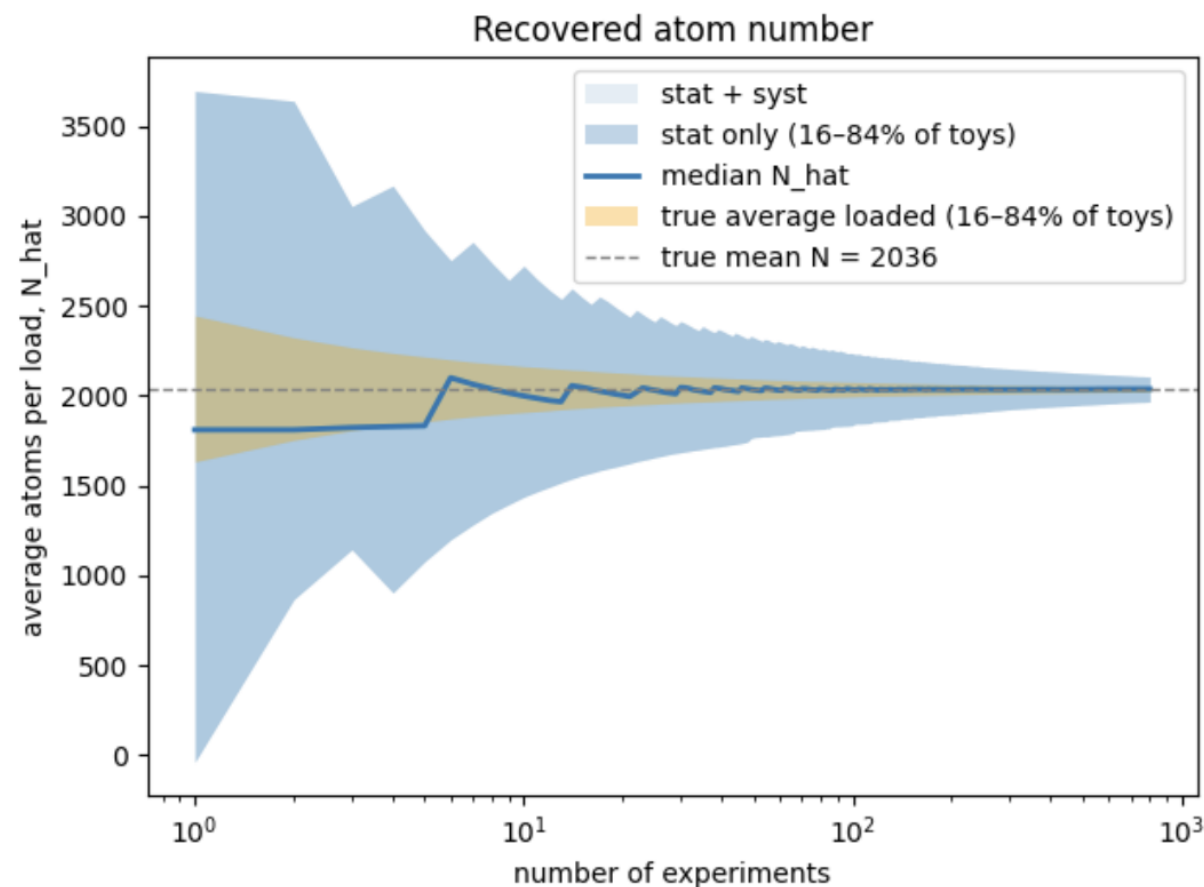
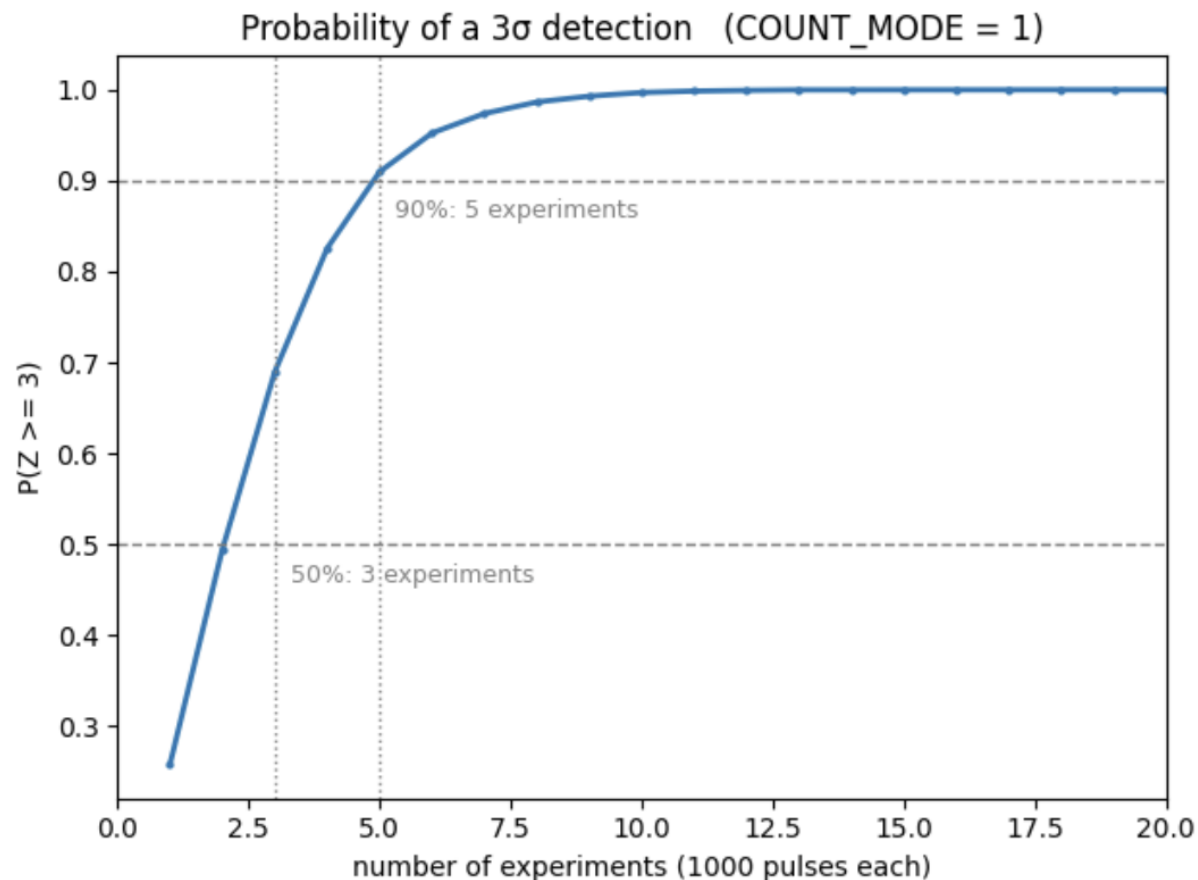


SiPM in HAICU (Zach)

Monte Carlo simulation (preliminary results):

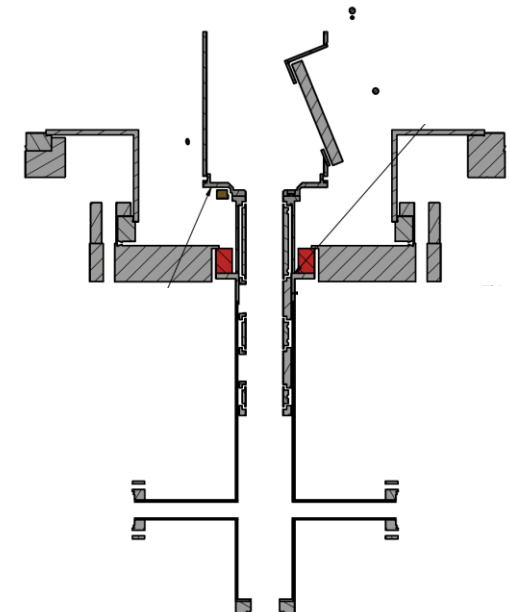
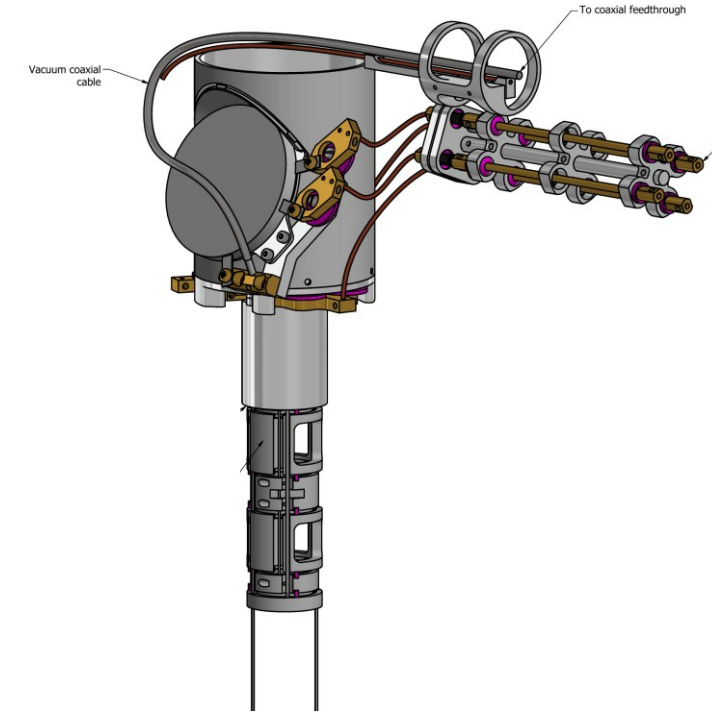
Define an “experiment” as 1000 laser pulses (50Hz laser → 20 seconds of exposure time)

- We require 5 experiments to get a 90% chance of a 3 sigma detection of atoms in the trap (subject to change as we hone in the parameters input into the sim)



MCP front (Chukman)

- Proton detection needs guiding electric field.
- Simultaneous detection of VUV and proton incompatible with laser cooling.
 - But it's advantageous to get both
- Proton-only detection compatible with on-axis laser
 - Proton collection efficiency ~22% (twice as VUV)
- TBD: 243nm port and ionization scheme?



Summary

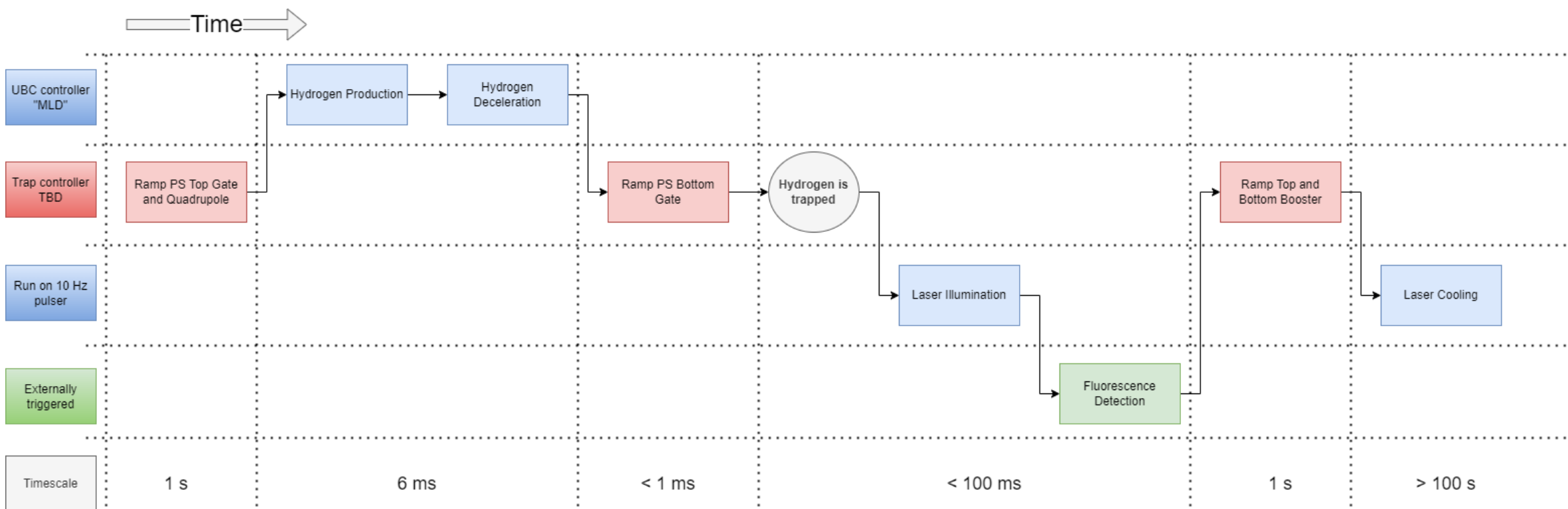
- CS is fully deployed; additional features are being added.
- 2/3 detectors are ready.

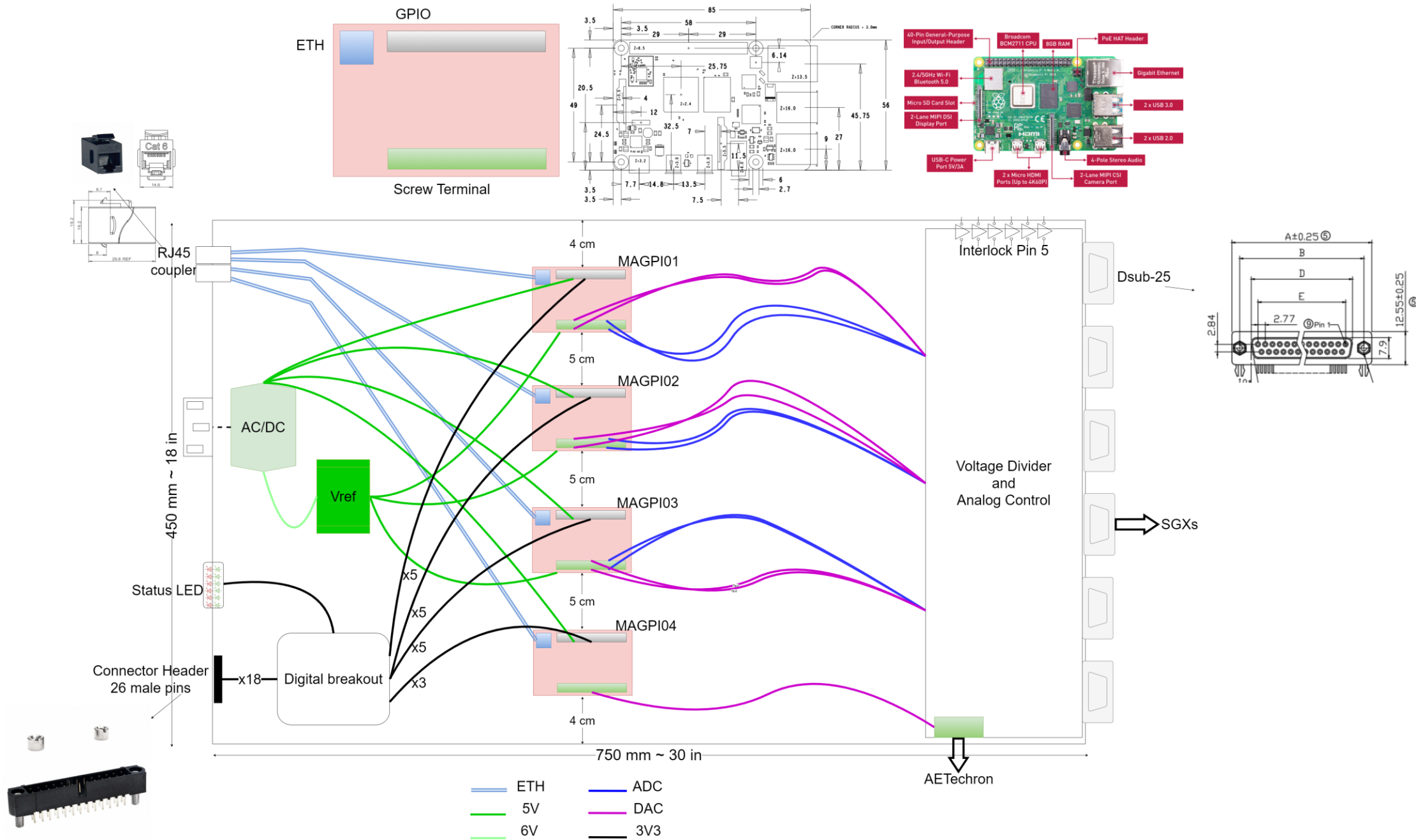
Thank you
Merci

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Firmware Changes (ppg_cb_firmware)

Event logger and FIFO

Added the Chronobox event logger (cb_main.v) module back into the firmware and linked it to a FIFO queue (fifo.v) module which the HPS accesses from address 0x20000. Also added a synchronized reset into cb_main.

Register map

Register 18 (read only) contains the FIFO status.
Registers 19-26 modify per-channel leading edge (19-22) and trailing edge (23-26) bit masks.

Software Changes (ppg_client)

TimestampFifo class

Added a TimestampFifo class (header and source) which handles hardware interaction for reading and writing to the FPGA memory.

MIDAS equipment

Added a new equipment to the ppg MIDAS client which handles all integration of the new event logging system.

MIDAS banks

FIFO data sent in two MIDAS banks in the SYSTEM buffer, TSEN and TSDE which offer two different encodings of the event data.

ODB settings

ODB settings allow configuration of LE and TE masks, toggling TSEN and TSDE banks, minimum MIDAS event size, enabling MIDAS messages, and pin naming.

Timestamp Event Encoding

TSEN (timestamp encoded)

TSEN uses 32-bit words and is the raw data the FPGA outputs, which requires a lot of logic to decode into meaningful information. It sends a wrap event every 0.839 seconds to signify the high precision timer has overflowed and requires parity logic to handle race conditions with these wrap events and regular data events.

TSDE (timestamp decoded)

TSDE uses 64-bit words and internally handles all the decode logic to get the total runtime. It outputs the data using one leading edge bit, 7 channel bits, and 56 bits of raw nanoseconds. This bank is much easier to use but requires twice the data per event.

The next slides will show an example of how encoding / decoding works for each of these banks.

Timestamp Event Decoding Example: TSEN

TSEN wrap event: 11111111 00000100 01101001 11110110

starts with 11111111 or 0xFF

parity bit

wrap count (one behind)

Each wrap occurs after 2^{23} increments of 100 ns so this wrap corresponds to a runtime of 242657.263616 seconds (about 2.8 days).

TSEN data event: 10011001 10001000 10101100 10100110

always 1

channel bits

parity bit

timestamp (200ns)

TE bit

Parity mismatch: this data event had a race condition with the wrap event and got sent before the wrap even though it took place after, correcting this means adding one to the wrap counter before getting the timestamp for this event.

Note: the internal counter operates on 100ns ticks, but the lowest bit holds the TE flag, so the timer resolution is 200ns

This event corresponds to channel 25 with a leading edge at a runtime of 242658.159325400 seconds.

Timestamp Event Decoding Example: TSDE

TSDE event: 10011001 00000000 11011100 10110010
 01000001 01100011 01110000 11011000

LE bit
channel bits
timestamp (ns)

This corresponds to channel 25 with a leading edge at a runtime of 242658.159325400 seconds (same as last slide).

This bank is very convenient to use since it only requires a few bit masks to extract the data.

Timing Analysis

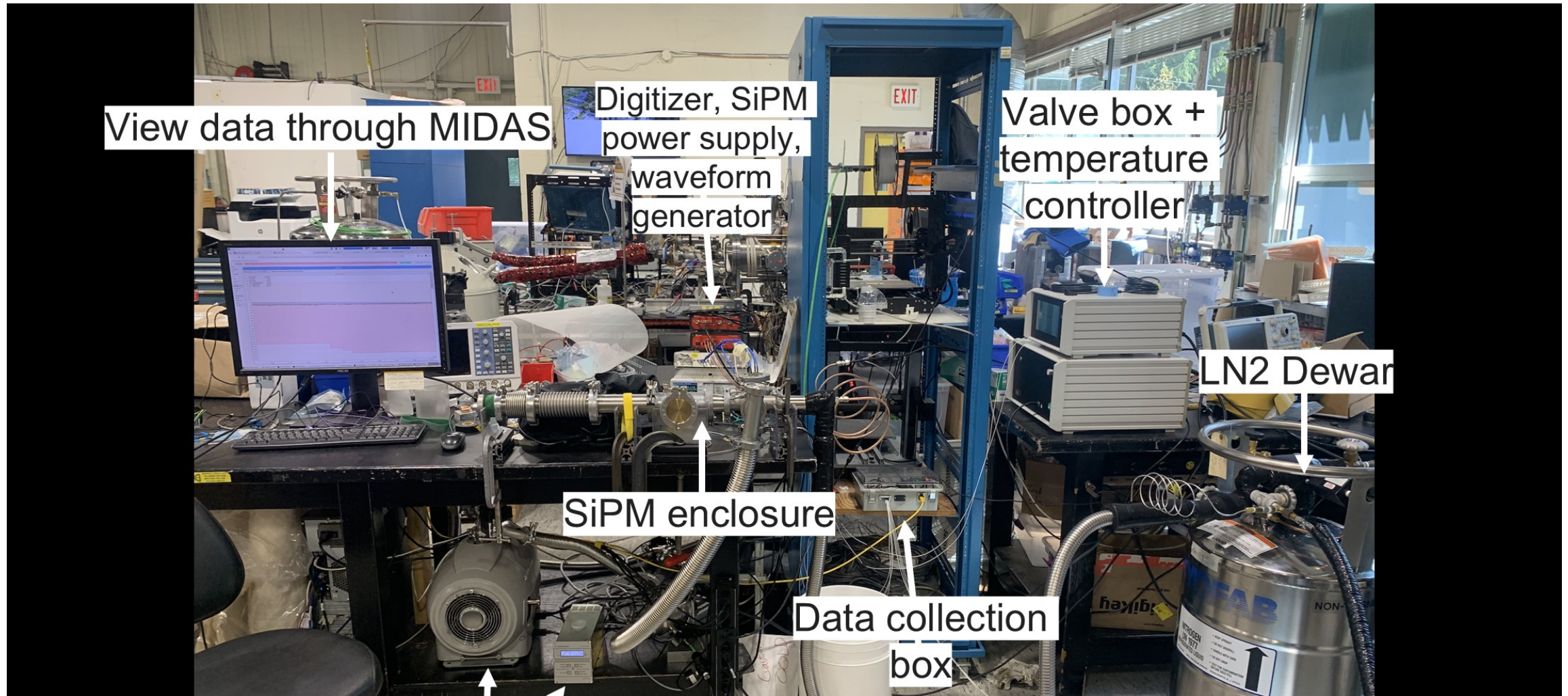
Log Precision & Accuracy

Using a function generator and an oscilloscope along with a PPG programming cycle, the log timing was checked against the physical outputs. The logs have $\pm 200\text{ns}$ precision, so given a $1\mu\text{s}$ long pulse, logs showed 800ns to 1200ns lengths. Logs also show zero delay between external trigger, and the start of the first pulse, even though the actual delay is approximately $100\text{-}130\text{ns}$.

Time Keeping

The logs kept time well even after leaving the PPG running for multiple days, showing the decoding is working properly. The logs were also consistent in their timing, meaning the parity logic was also working correctly (logs would jump ahead and behind by 0.839 seconds if improperly decoded).

SiPM test setup (Zach)



Data

- Digitizer chan.s assignment

1. PMT Excitation
2. PMT Emission (commissioning)?
3. MCP front
4. MCP side
5. SiPM 0
6. SiPM 1
7. SiPM 2
8. SiPM 3

- Max trigger rate: 50 Hz
- Acquisition window: 2 us (max)
 - The shorter, the better
 - Number of samples: 1000 samples
 - Waveform size: 2kB
- Data rate: $8 \times 2\text{kB} \times 50 = 800 \text{ kB/s}$